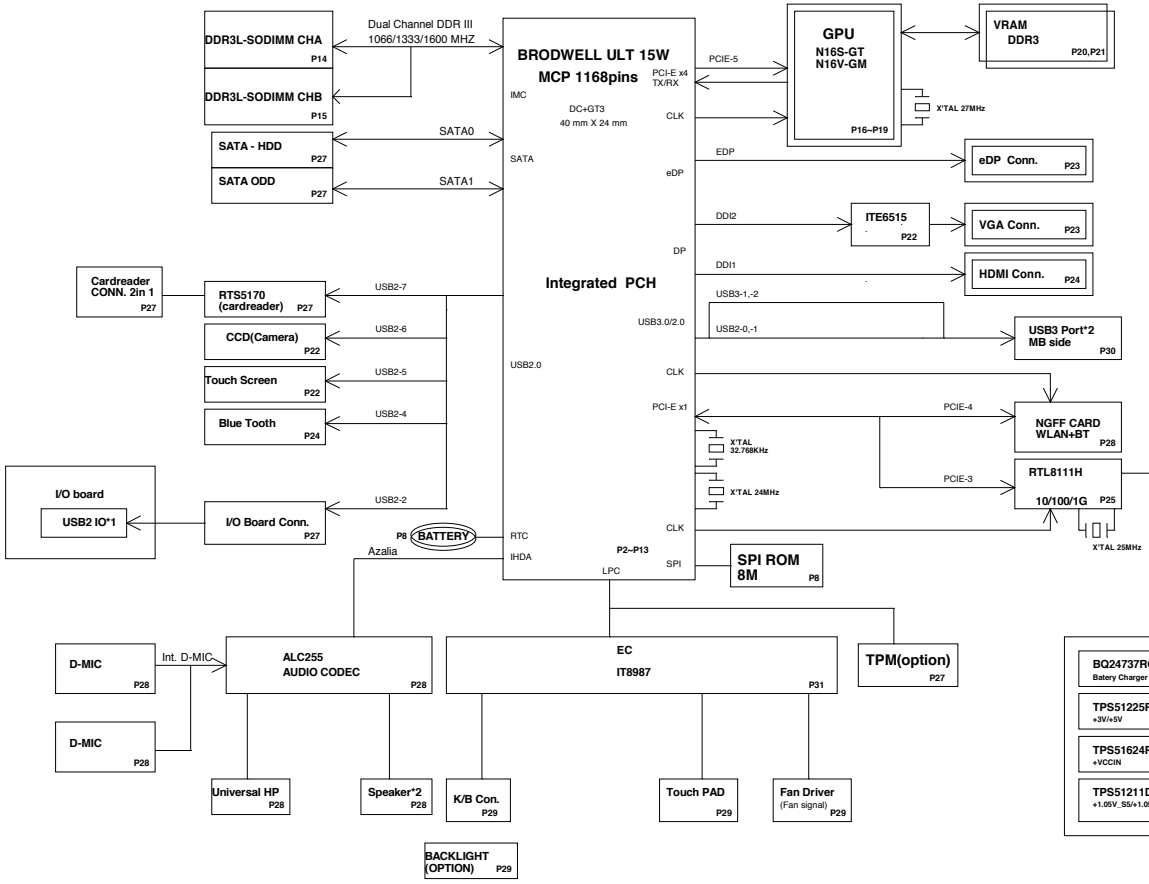
ZRT/ZRTA_GDDR3 BWD ULT SYSTEM BLOCK DIAGRAM



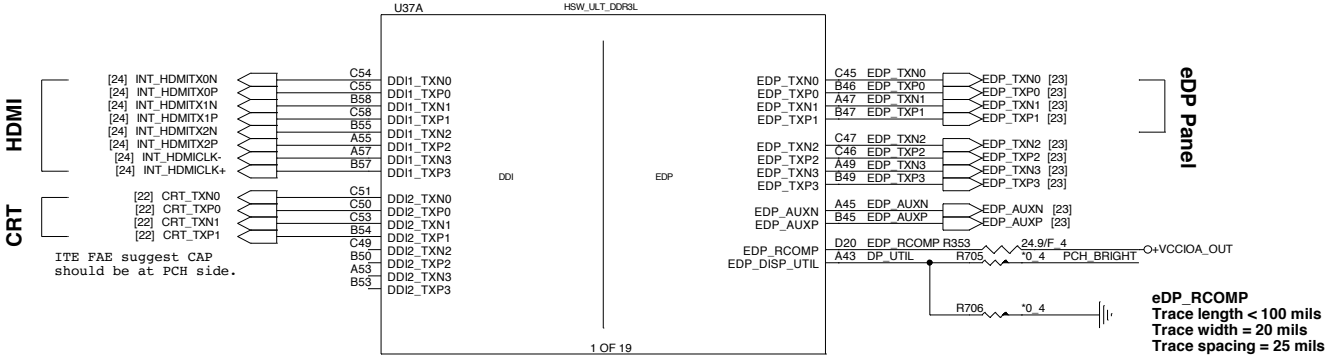
BOM

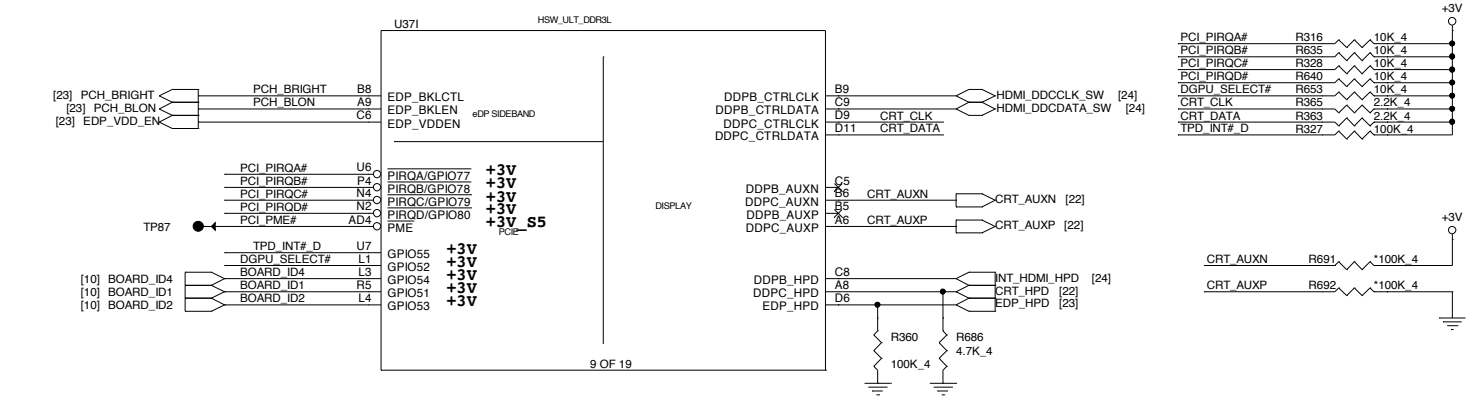
15@ : For 15W CPU
28@ : For 28W CPU
6515@ : For 6515 stuff
AC@ : For IOAC
DM@ : Dual MIC
DR@ : For Dual Rank
EV@ : Optimus
GM@ :N16V-GM /WO GC6
GS@ : G sensor
GT@ :N16S-GT /GC6
IV@ : iGPU
KBL@ : Keyboard backlight
NAC@ : Non IOAC
NGS@ : Non G sensor
NTPM@ : Non TPM
S28@ : 28W Change BOM
SM@ : Single MIC
SP@ : Special
SR@ : Single Rank
TPM@ : TPM
TPN_N@ : For TPM 2.0
TPN_S@ : For TPM 1.2

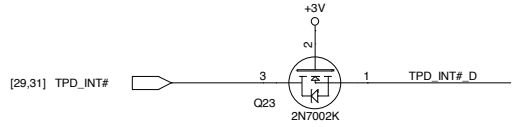
BQ24737RGRR Batery Charger	P31	TPS51216RUKR +1.35V_SUS	P35	Thermal Protection Discharger	P36
TPS51225RUKR +3V/+5V	P32	TPS54318RTER +1.5V	P36		
TPS51624RSM +VCCIN	P33	UP1658RQKF +VGPU_CORE	P37		
TPS51211DSCR +1.05V_S5/+1.05V	P34	PS51211DSCR +1.5V_GFX/1.05V_GFX/3V_GFX	P38		

Quanta Computer Inc.
PROJECT : ZRT/ZRTA
Block Diagram
Rev 3A
Date: Wednesday, February 11, 2015 Sheet 1 of 44

Haswell ULT (DISPLAY,eDP)



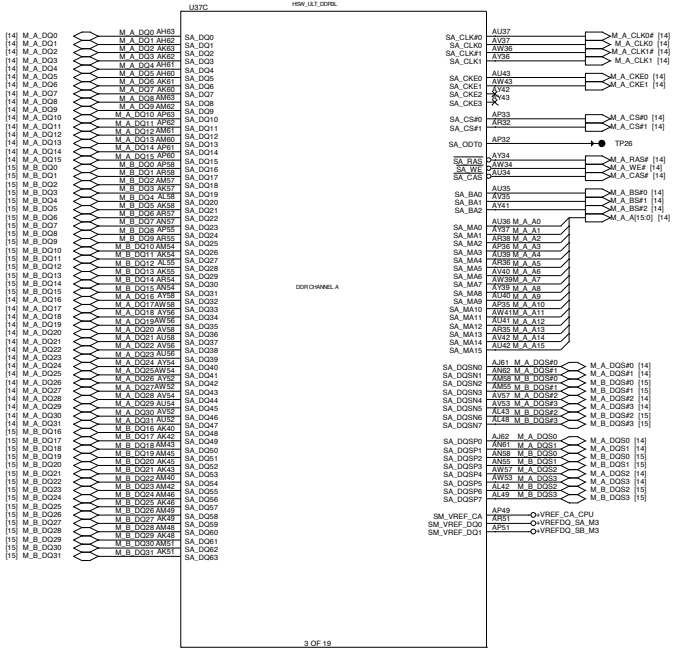




Quanta Computer Inc.		
PROJECT : ZRT/ZRTA		
Size	Document Number: Haswell 3/5 (DDI/eDP)	Rev 3A
Date: Wednesday, February 11, 2015	Sheet 2 of 44	

Change Data and DQS to interleave.

Haswell ULT (DDR3L)



Haswell Processor (DDR3)

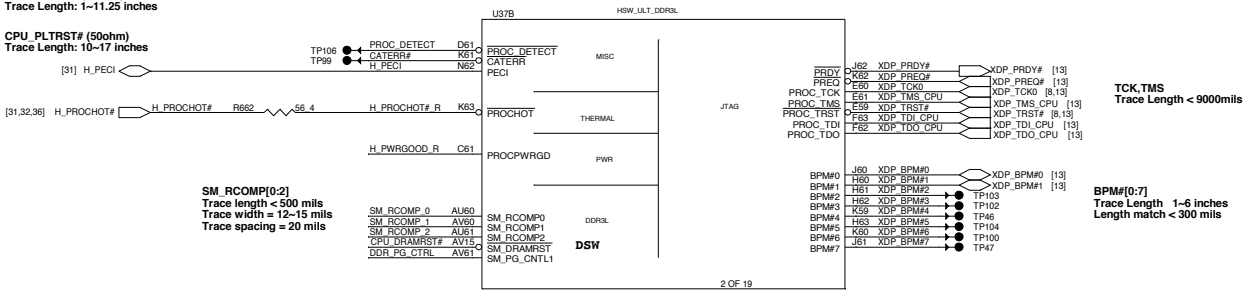
Quanta Computer Inc.		
PROJECT : ZRT/ZRTA		
Size	Document Number: Haswell 2/5 (DDR3 I/F)	Rev: 3A
Date: Wednesday, February 11, 2015	Sheet 3 of 44	

Haswell ULT (SIDEBAND)

H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 iches

H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches

CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches

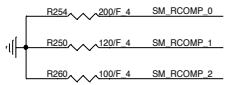


SM_RCOMP[0:2]
Trace length < 500 mils
Trace width = 12~15 mils
Trace spacing = 20 mils

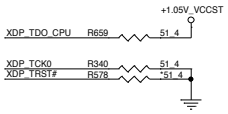
TCK,TMS
Trace Length < 9000mils

BPM#[0:7]
Trace Length 1~6 inches
Length match < 300 mils

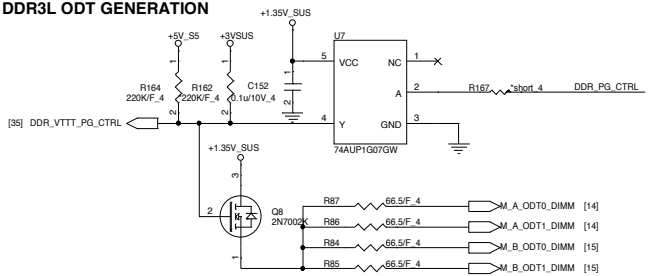
DRAM COMP



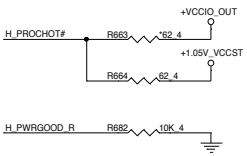
XDP PU/PD



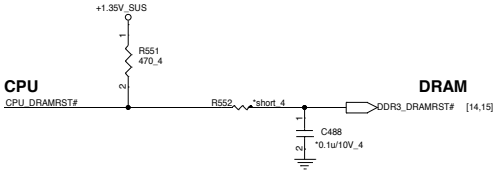
DDR3L ODT GENERATION



PU/PD of CPU



DRAMRST



Quanta Computer Inc.		
PROJECT : ZRT/ZRTA		
Size	Document Number	Rev
	Haswell 1/5 (PEG/DMI/FDI)	3A
Date: Wednesday, February 11, 2015	Sheet 4 of 44	

Haswell ULT (POWER)

VDDQ Output Decoupling Recommendations		
330uFx2	7343	BOT socket side
22uFx11	0805	5 onTOP, 6 on BOTTOM inside socket cavity
10uFx10	0805	5 onTOP, 5 on BOT inside socket cavity

VCC Output Decoupling Recommendations		
470uFx4	7343	TOP socket side
22uFx8	0805	4 on TOP, 4 on BOT near socket edge
22uFx11	0805	TOP, inside socket cavity
10uFx1	0805	BOT, inside socket cavity

VCCST PWRGD

CRB is via +1.05V PG

Reserve from EC

1A-6 2013/10/21 Del APWORK.

SVID

Layout note: need routing together and ALERT need between CLK and DATA.

Place PU resistor close to CPU

Place PU resistor close to CPU

HWPG_1.05V for DDR=1.5V

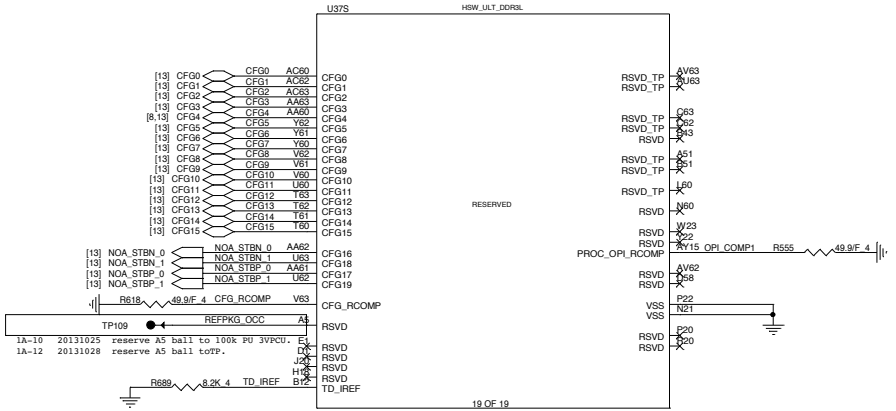
10/30 reserve
DDR=1.5V ,This block POP

Quanta Computer Inc.
PROJECT : ZRT/ZRTA

Size	Document Number	Rev
	Haswell 4/5 (POWER)	3A

Date: Wednesday, February 11, 2015 Sheet 5 of 44

Haswell ULT (CFG,RSVD)

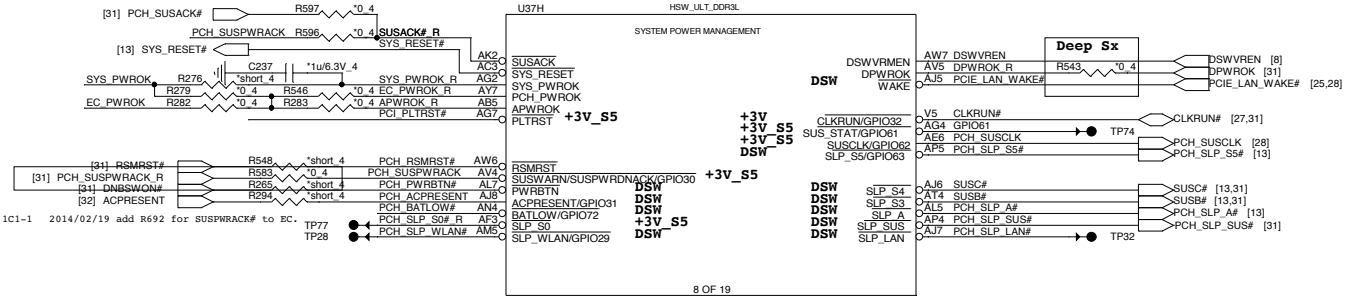


Processor Strapping

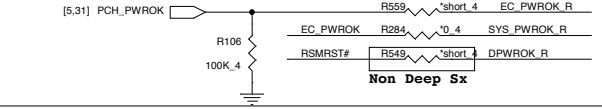
	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	**(DEFAULT) NORMAL OPERATION; NO STALL**	STALL	CFG0 R289 *1K_4
CFG1 PCH/ PCH LESS MODE SELECTION	**(DEFAULT) NORMAL OPERATION**	PCH-LESS MODE	CFG1 R606 *1K_4
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	**DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT**	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG3 R610 *1K_4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	**DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS**	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG8 R614 *1K_4
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	**VRS SUPPORTING SVID PROTOCOL ARE PRESENT**	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R619 *1K_4
CFG10 SAFE MODE BOOT	**POWER FEATURES ACTIVATED DURING RESET**	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R295 *1K_4

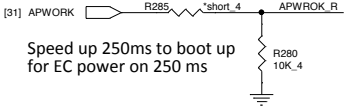
Quanta Computer Inc.
PROJECT : ZRT/ZRTA
Size | Document Number: Haswell 5/5 (CFG/GND) | Rev: 3A
Date: Wednesday, February 11, 2015 | Sheet 6 of 44

Haswell ULT PCH (PM)

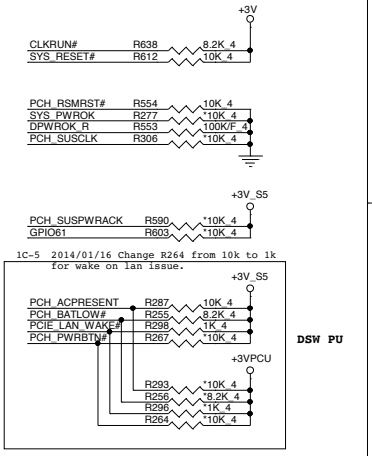


Power Sequence

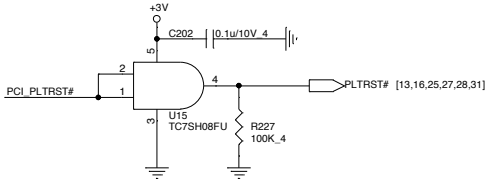




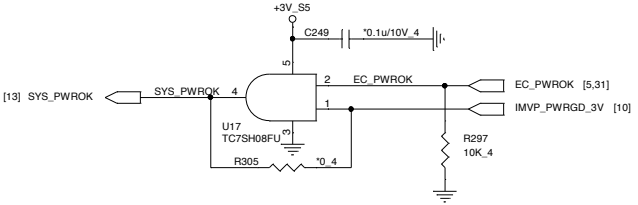
PCH PM PU/PD



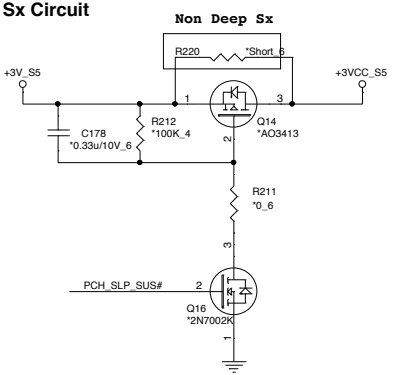
PLTRST# Buffer



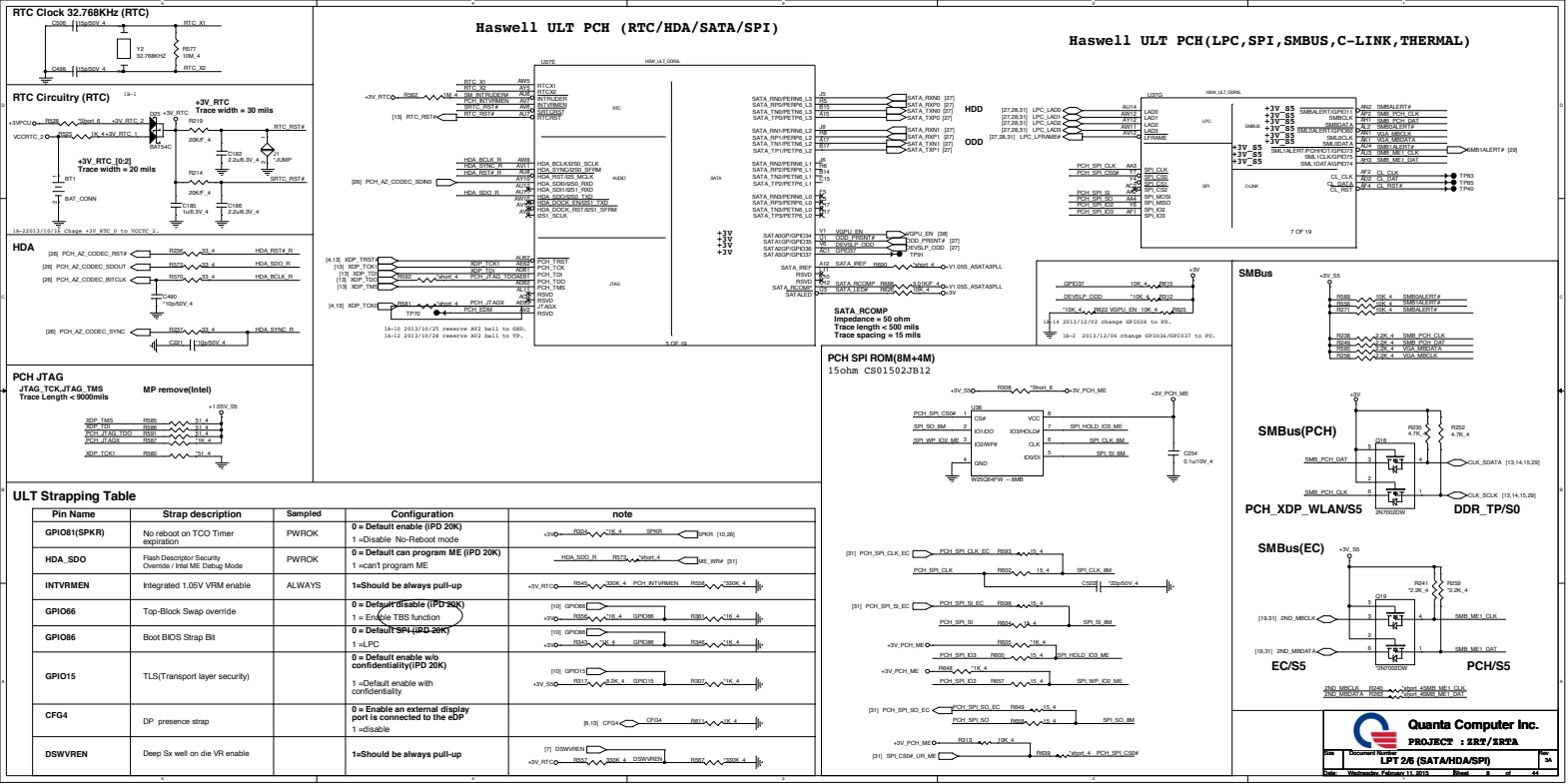
SYSPWOK



Deep Sx Circuit



Quanta Computer Inc.		
PROJECT : ZRT/ZRTA		
Size	Document Number: LPT 1/6 (DMI/FDI/VGA)	Rev 3A
Date: Wednesday, February 11, 2015	Sheet 7 of 44	



ULT Strapping Table

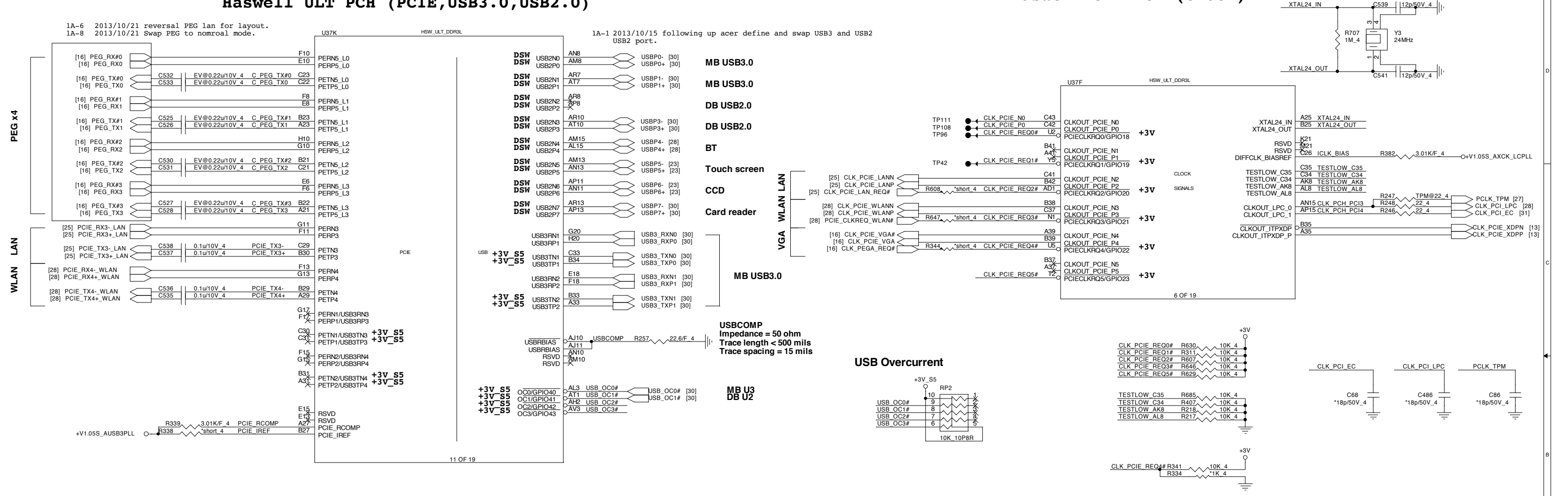
Pin Name	Strap description	Sampled	Configuration	note
GPIO81(SPKR)	No reboot on TCO Timer expiration	PWROK	0 = Default enable (iPD 20K) 1 =Disable No-Reboot mode	
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Default can program ME (iPD 20K) 1 =can't program ME	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	1=Should be always pull-up	
GPIO66	Top-Block Swap override		0 = Default disable (iPD 20K) 1 = Enable TBS function	
GPIO86	Boot BIOS Strap Bit		0 = Default SPI (iPD 20K) 1 =LPC	
GPIO15	TLS(Transport layer security)		0 = Default enable w/o confidentiality(iPD 20K) 1 =Default enable with confidentiality	
CFG4	DP presence strap		0 = Enable an external display port is connected to the eDP 1 =disable	
DSWVREN	Deep Sx well on die VR enable		1=Should be always pull-up	

Haswell ULT PCH (PCIE,USB3.0,USB2.0)

1A-6 2013/10/21 reversal PEG lan for layout.
1A-8 2013/10/21 Swap PEG to nomroal mode.

1A-1 2013/10/15 following up acer define and swap USB3 and USB2
USB2 port.

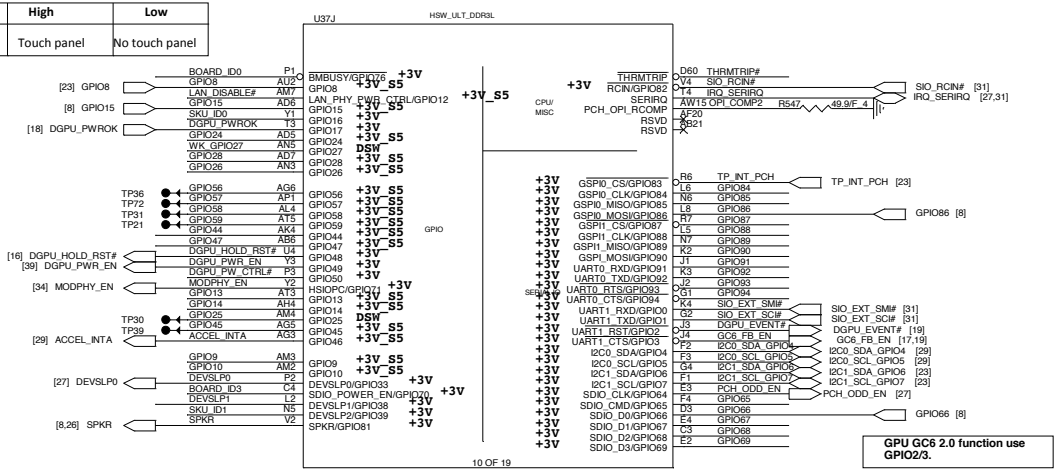
Haswell ULT PCH (CLOCK)



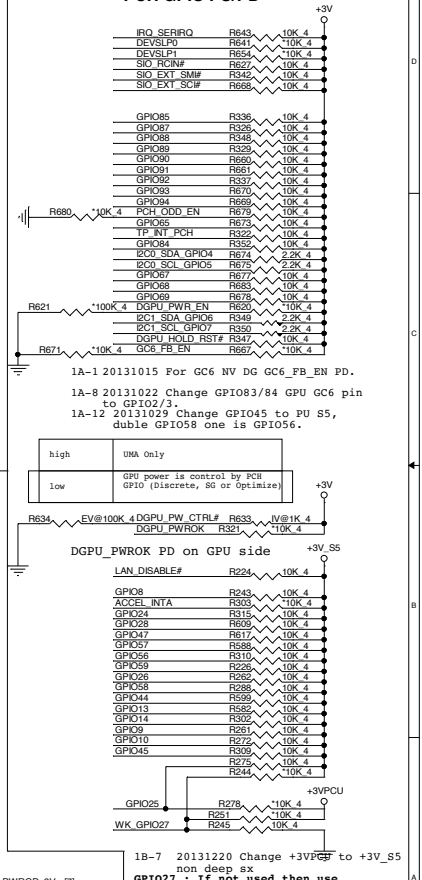
Quanta Computer Inc.		
PROJECT : ZRT/ZRTA		
Size	Document Number: LPT 3/6 (PCIE/USB/CLK)	Rev 3A
Date: Wednesday, February 11, 2015	Sheet 9 of 44	

Haswell ULT PCH (GPIO,CPU/MISC,NCTF)

	High	Low
GPIO8	Touch panel	No touch panel

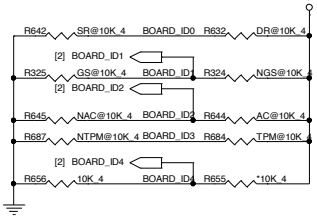


PCH GPIO PU/PD



high	UMA Only
low	GPU power is control by PCH GPIO (Discrete, SG or Optimize)

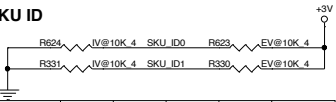
Board ID



	Low	High
BOARD_ID0	single rank SKU	Dual rank SKU
BOARD_ID1	Reserved (Default)	Reserve
BOARD_ID2	No IOAC	IOAC
BOARD_ID3	No TPM	TPM
BOARD_ID4	Non-Dolly (Default)	Dolly

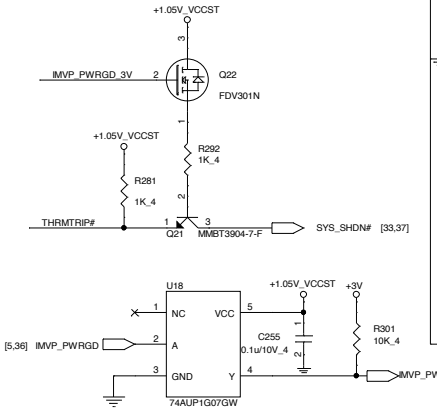
RAM ID

SKU ID



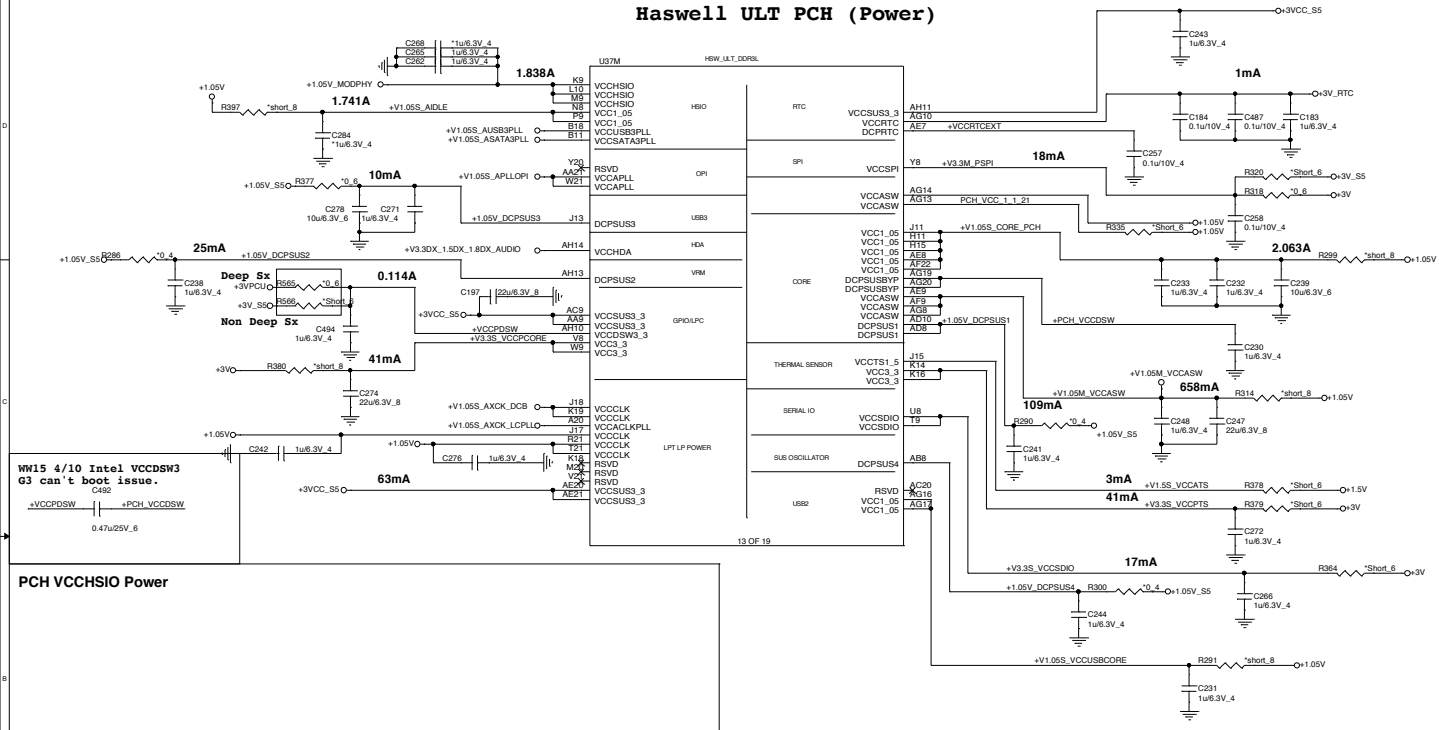
	SKU_ID1	SKU_ID0	VGA H/W Signal	Setup Menu	
UMA Only	0	0	UMA	Hidden	UMA boot
dGPU Only	0	1	GPU	Hidden	GPU boot
Switchable (Mux)	1	0	UMA+GPU	dGPU/SG	UMA boot
Optimize (Muxless)	1	1	UMA	UMA/SG	UMA boot

CPU thermal trip

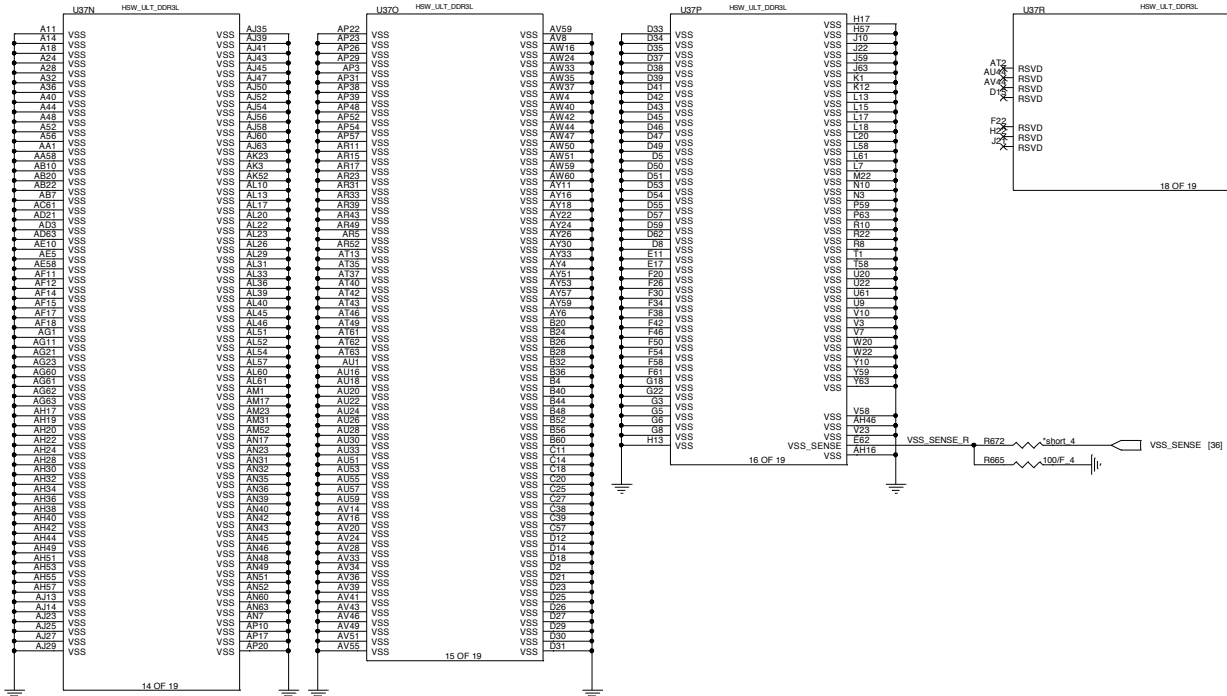


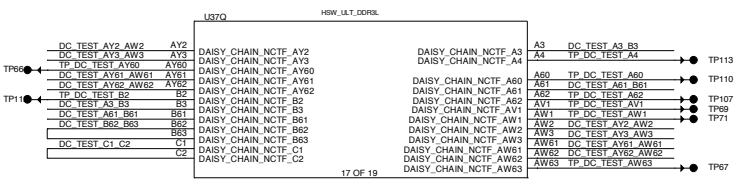
Quanta Computer Inc.
PROJECT : ZRT/ZRTA
Size: Document Number: LPT 4/6 (GPIO/MISC) Rev: 3A
Date: Wednesday, February 11, 2015 Sheet 10 of 44

Haswell ULT PCH (Power)

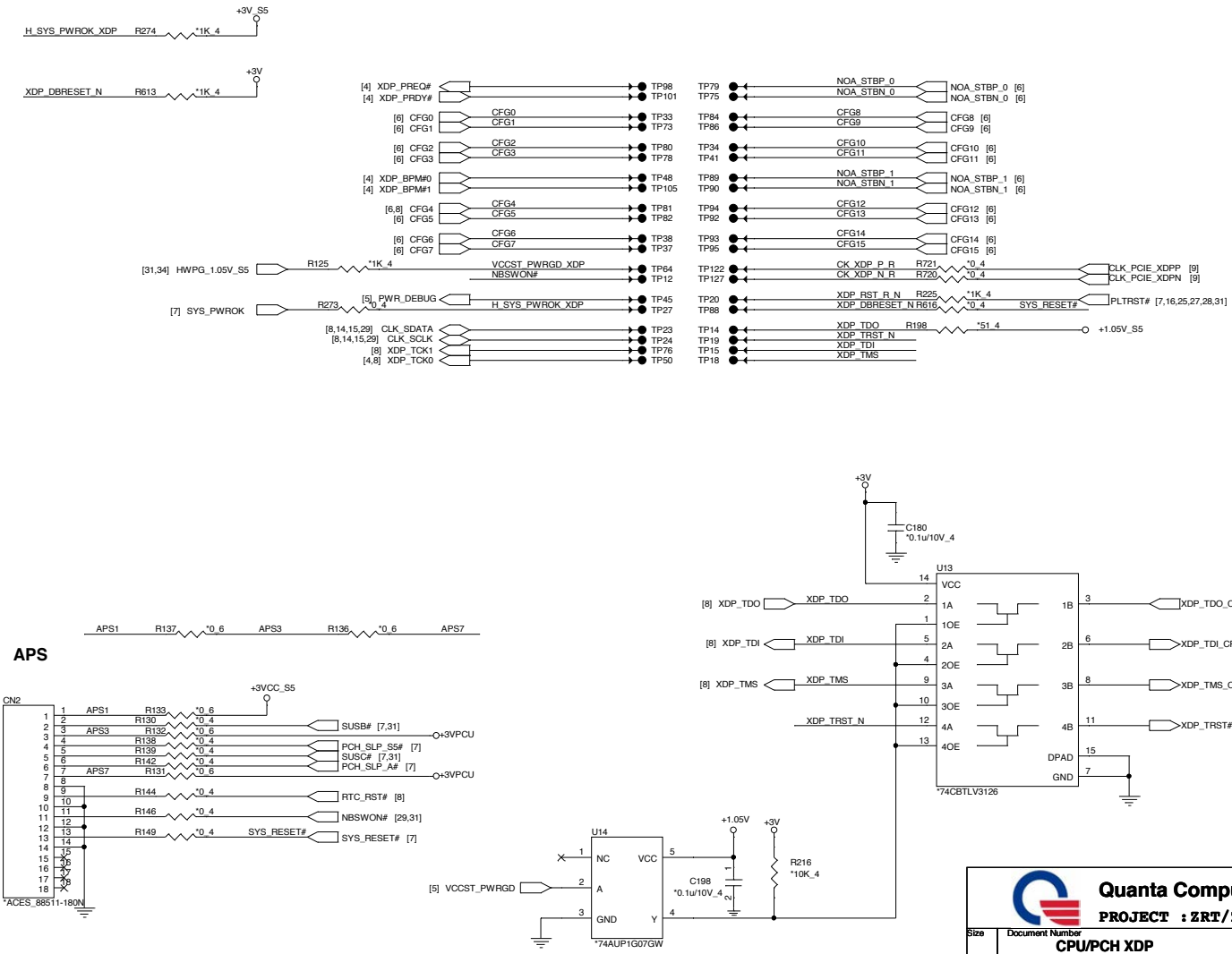


Haswell ULT (GND)





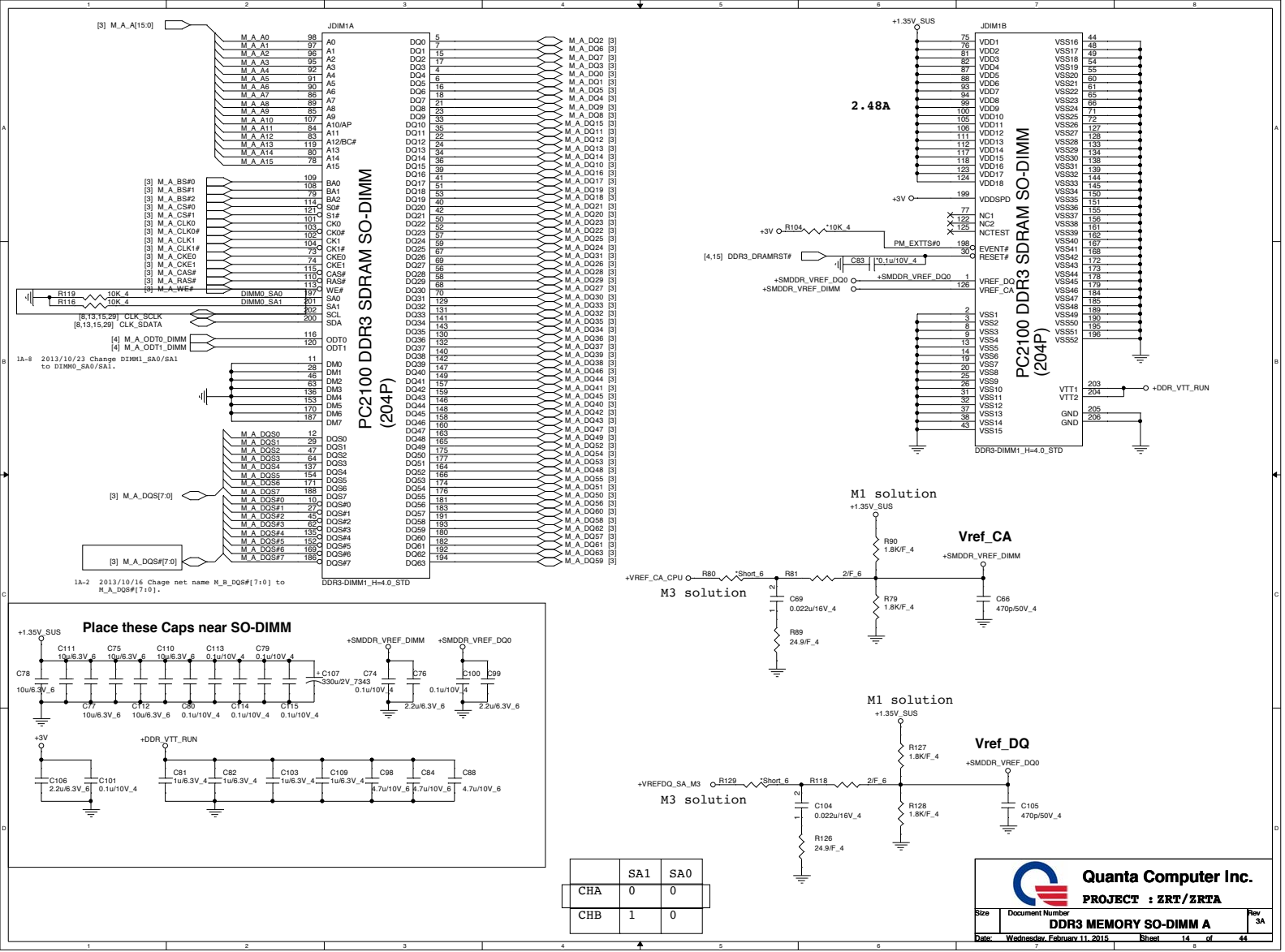
Quanta Computer Inc.		
PROJECT : ZRT/ZRTA		
Size	Document Number	Rev
	LPT 6/6 (GND)	3A
Date: Wednesday, February 11, 2015	Sheet 12 of 44	



APS

APS1 R137 *0_6 APS3 R136 *0_6 APS7

Quanta Computer Inc.			
PROJECT : ZRT/ZRTA			
Size	Document Number		Rev
	CPU/PCH XDP		3A
Date: Wednesday, February 11, 2015	Sheet 13 of 44		



	SA1	SA0
CHA	0	0
CHB	1	0

Quanta Computer Inc.

PROJECT : ZRT/ZRTA

Size	Document Number	Rev
	DDR3 MEMORY SO-DIMM A	3A

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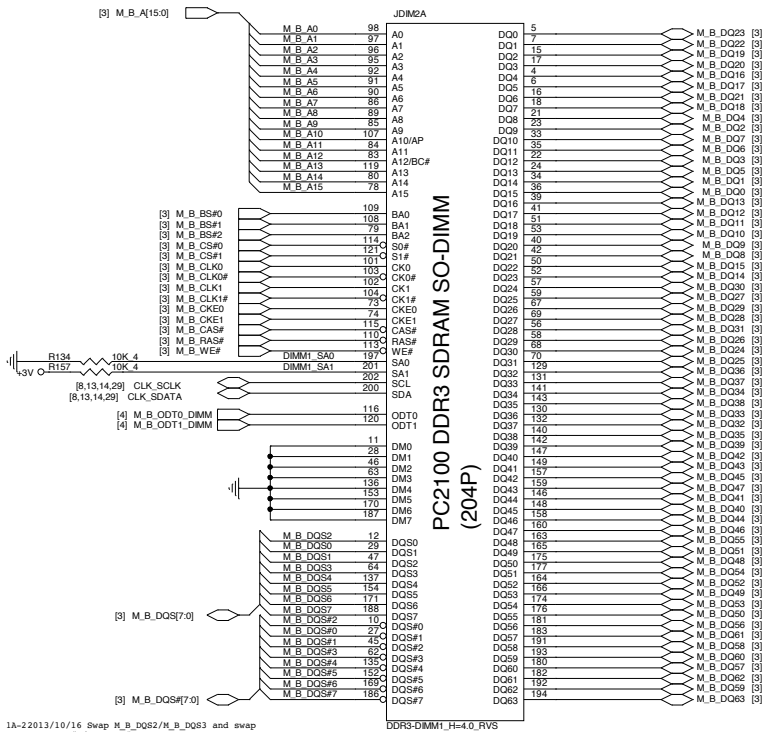

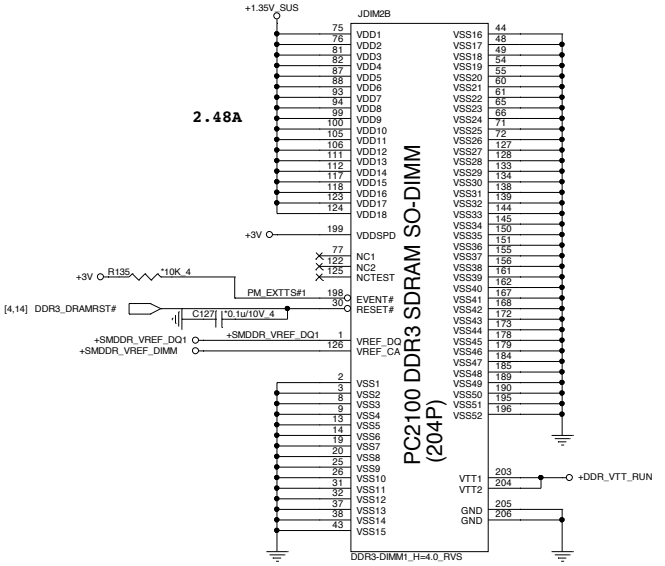

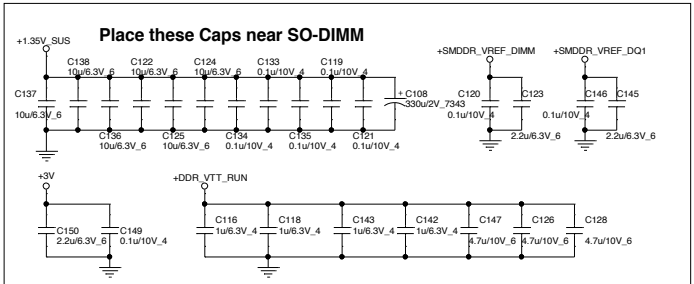

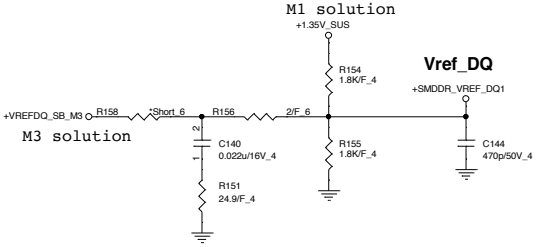

	SA1	SA0
CHA	0	0
CHB	1	0

Quanta Computer Inc.

PROJECT : ZRT/ZRTA

Size	Document Number	Rev
	DDRIII Memory SO-DIMM B	3A

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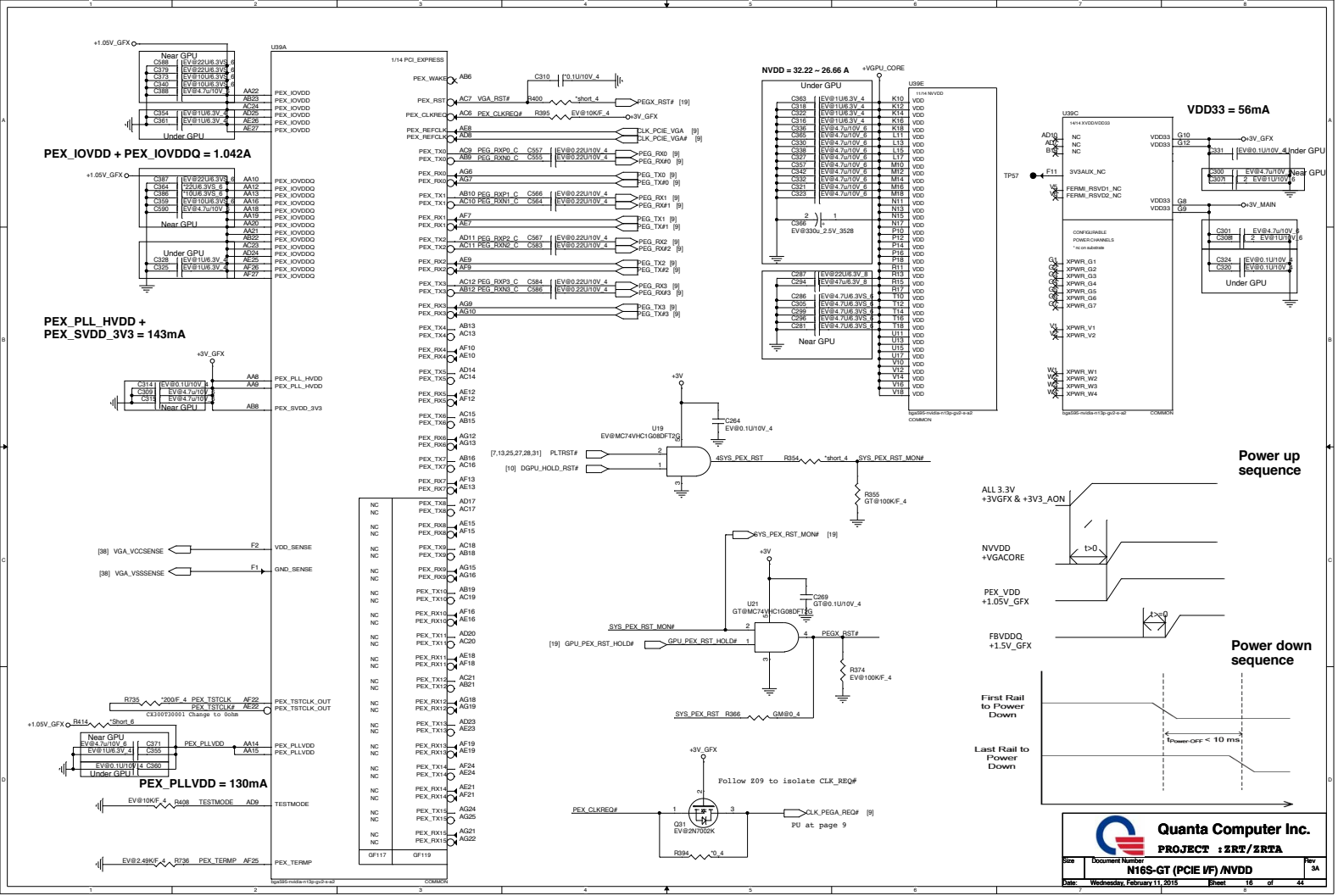
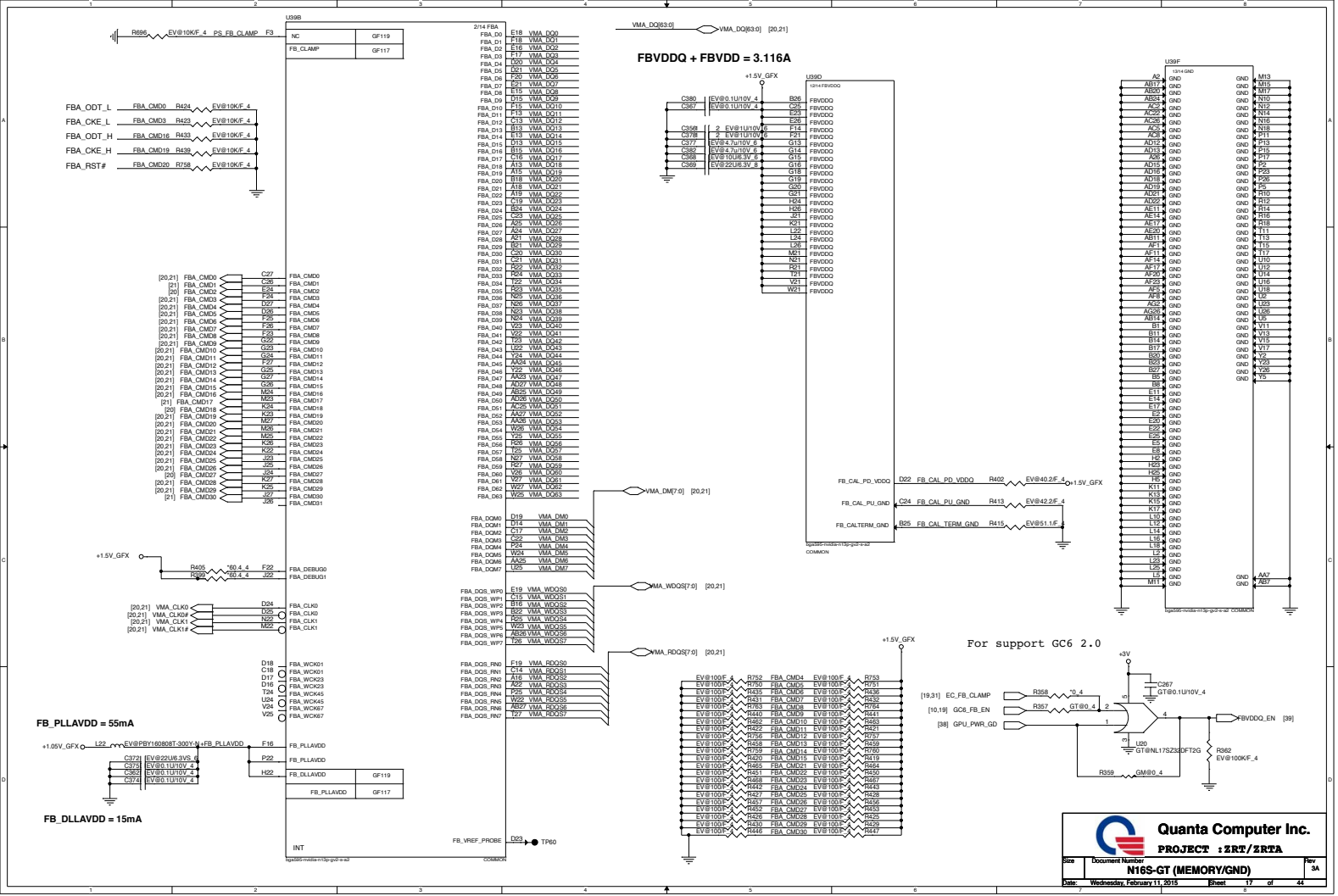
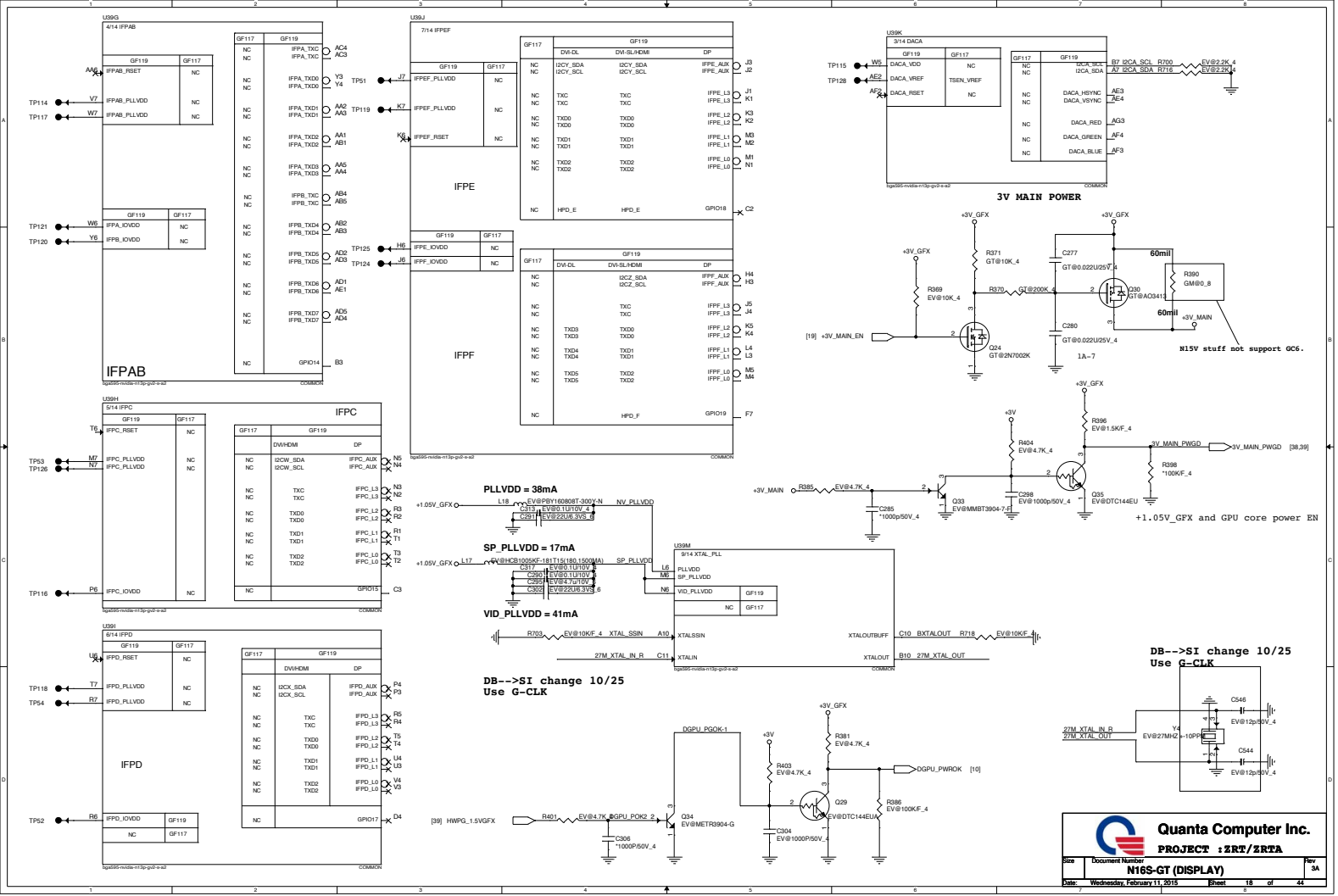
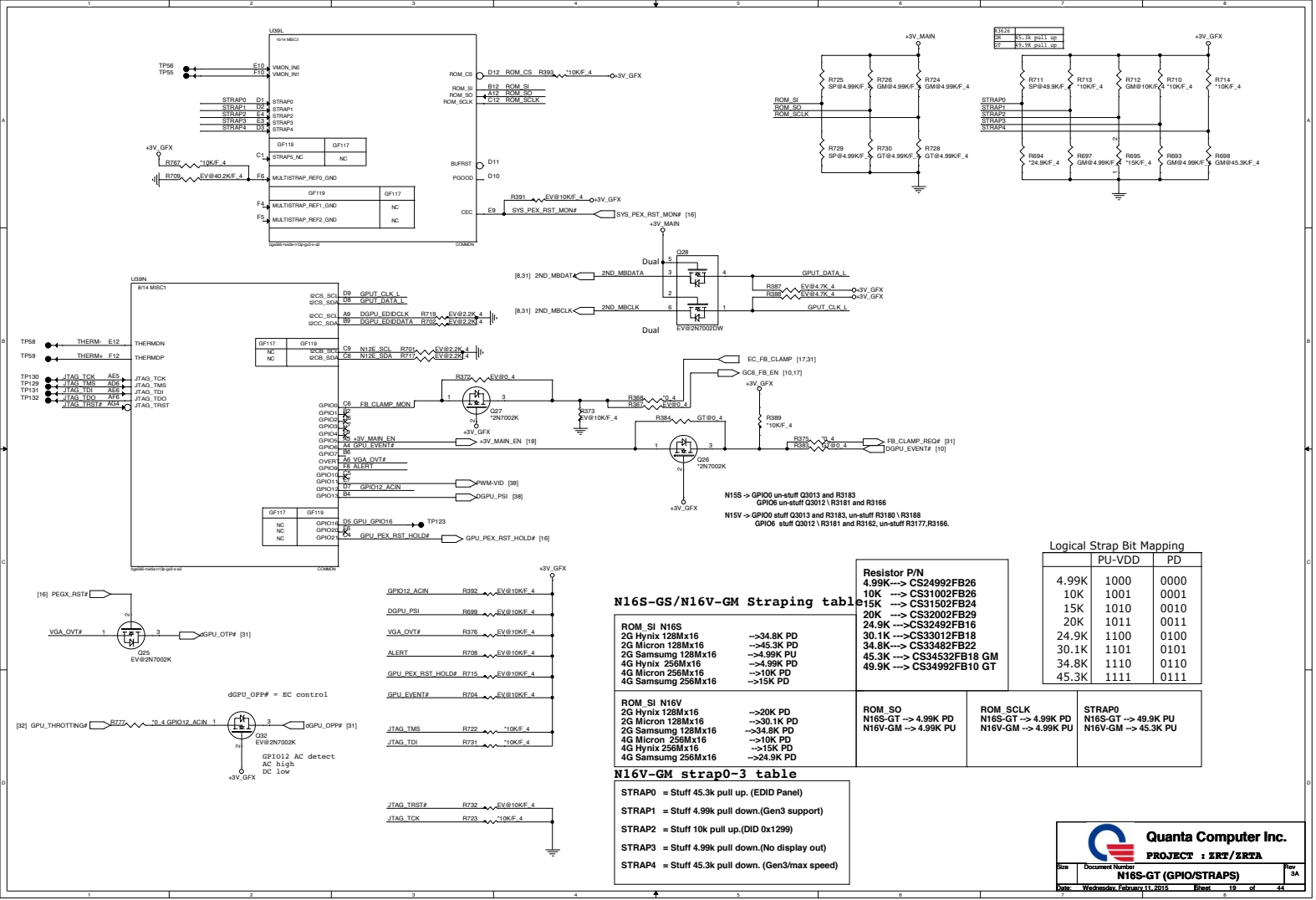

PEX_IOVDD + PEX_IOVDDQ = 1.042A
PEX_PLL_HVDD + PEX_SVDD_3V3 = 143mA
PEX_PLLVDD = 130mA
NVDD = 32.22 ~ 26.66 A
VDD33 = 56mA
Power up sequence
Power down sequence
ALL 3.3V +3VGFX & +3V3_AON
NVVDD +VGACORE
PEX_VDD +1.05V_GFX
FBVDDQ +1.5V_GFX
First Rail to Power Down
Last Rail to Power Down
Follow Z09 to isolate CLK_REQ#
Quanta Computer Inc.
PROJECT : ZRT/ZRTA
N16S-GT (PCIE I/F) /NVDD
Wednesday, February 11, 2015


U39B
R696 EV@10K/F_4 PS_FB_CLAMP F3
NC GF119
FB_CLAMP GF117
FBA_ODT_L FBA_CMD0 R424 EV@10K/F_4
FBA_CKE_L FBA_CMD3 R423 EV@10K/F_4
FBA_ODT_H FBA_CMD16 R433 EV@10K/F_4
FBA_CKE_H FBA_CMD19 R439 EV@10K/F_4
FBA_RST# FBA_CMD20 R758 EV@10K/F_4
2/14 FBA
FBA_D0 E18 VMA_DQ0
FBA_D1 F18 VMA_DQ1
FBA_D2 E16 VMA_DQ2
FBA_D3 F17 VMA_DQ3
FBA_D4 D20 VMA_DQ4
FBA_D5 D21 VMA_DQ5
FBA_D6 F20 VMA_DQ6
FBA_D7 E21 VMA_DQ7
FBA_D8 E15 VMA_DQ8
FBA_D9 D15 VMA_DQ9
FBA_D10 F15 VMA_DQ10
FBA_D11 F13 VMA_DQ11
FBA_D12 C13 VMA_DQ12
FBA_D13 B13 VMA_DQ13
FBA_D14 E13 VMA_DQ14
FBA_D15 D13 VMA_DQ15
FBA_D16 E15 VMA_DQ16
FBA_D17 C16 VMA_DQ17
FBA_D18 A13 VMA_DQ18
FBA_D19 A15 VMA_DQ19
FBA_D20 B18 VMA_DQ20
FBA_D21 A18 VMA_DQ21
FBA_D22 A19 VMA_DQ22
FBA_D23 C19 VMA_DQ23
FBA_D24 B24 VMA_DQ24
FBA_D25 C23 VMA_DQ25
FBA_D26 A25 VMA_DQ26
FBA_D27 A24 VMA_DQ27
FBA_D28 A21 VMA_DQ28
FBA_D29 B21 VMA_DQ29
FBA_D30 C20 VMA_DQ30
FBA_D31 C21 VMA_DQ31
FBA_D32 B22 VMA_DQ32
FBA_D33 R24 VMA_DQ33
FBA_D34 T22 VMA_DQ34
FBA_D35 R23 VMA_DQ35
FBA_D36 N25 VMA_DQ36
FBA_D37 N26 VMA_DQ37
FBA_D38 N23 VMA_DQ38
FBA_D39 N24 VMA_DQ39
FBA_D40 Y23 VMA_DQ40
FBA_D41 Y22 VMA_DQ41
FBA_D42 T23 VMA_DQ42
FBA_D43 U22 VMA_DQ43
FBA_D44 Y24 VMA_DQ44
FBA_D45 AA24 VMA_DQ45
FBA_D46 Y22 VMA_DQ46
FBA_D47 AA23 VMA_DQ47
FBA_D48 AD27 VMA_DQ48
FBA_D49 AB25 VMA_DQ49
FBA_D50 AB26 VMA_DQ50
FBA_D51 AC25 VMA_DQ51
FBA_D52 AA27 VMA_DQ52
FBA_D53 AA26 VMA_DQ53
FBA_D54 W26 VMA_DQ54
FBA_D55 Y25 VMA_DQ55
FBA_D56 R26 VMA_DQ56
FBA_D57 T25 VMA_DQ57
FBA_D58 N27 VMA_DQ58
FBA_D59 R27 VMA_DQ59
FBA_D60 Y26 VMA_DQ60
FBA_D61 V27 VMA_DQ61
FBA_D62 W27 VMA_DQ62
FBA_D63 W25 VMA_DQ63
[20,21] FBA_CMD0 C27 FBA_CMD0
[21] FBA_CMD1 C26 FBA_CMD1
[20] FBA_CMD2 E24 FBA_CMD2
[20,21] FBA_CMD3 D27 FBA_CMD3
[20,21] FBA_CMD4 D24 FBA_CMD4
[20,21] FBA_CMD5 D26 FBA_CMD5
[20,21] FBA_CMD6 F25 FBA_CMD6
[20,21] FBA_CMD7 F26 FBA_CMD7
[20,21] FBA_CMD8 F23 FBA_CMD8
[20,21] FBA_CMD9 G22 FBA_CMD9
[20,21] FBA_CMD10 G23 FBA_CMD10
[20,21] FBA_CMD11 G24 FBA_CMD11
[20,21] FBA_CMD12 F27 FBA_CMD12
[20,21] FBA_CMD13 G25 FBA_CMD13
[20,21] FBA_CMD14 G27 FBA_CMD14
[20,21] FBA_CMD15 G26 FBA_CMD15
[20,21] FBA_CMD16 M24 FBA_CMD16
[21] FBA_CMD17 M25 FBA_CMD17
[20] FBA_CMD18 K24 FBA_CMD18
[20,21] FBA_CMD19 K25 FBA_CMD19
[20,21] FBA_CMD20 M27 FBA_CMD20
[20,21] FBA_CMD21 M26 FBA_CMD21
[20,21] FBA_CMD22 M25 FBA_CMD22
[20,21] FBA_CMD23 K26 FBA_CMD23
[20,21] FBA_CMD24 K27 FBA_CMD24
[20,21] FBA_CMD25 J23 FBA_CMD25
[20,21] FBA_CMD26 J25 FBA_CMD26
[20] FBA_CMD27 J24 FBA_CMD27
[20,21] FBA_CMD28 K27 FBA_CMD28
[20,21] FBA_CMD29 K25 FBA_CMD29
[21] FBA_CMD30 J27 FBA_CMD30
J26 FBA_CMD31
FBA_DQM0 D19 VMA_DM0
FBA_DQM1 D14 VMA_DM1
FBA_DQM2 C17 VMA_DM2
FBA_DQM3 C22 VMA_DM3
FBA_DQM4 P24 VMA_DM4
FBA_DQM5 W24 VMA_DM5
FBA_DQM6 AA25 VMA_DM6
FBA_DQM7 U25 VMA_DM7
FBA_DQS_WP0 E19 VMA_WDQS0
FBA_DQS_WP1 C15 VMA_WDQS1
FBA_DQS_WP2 B16 VMA_WDQS2
FBA_DQS_WP3 B22 VMA_WDQS3
FBA_DQS_WP4 P25 VMA_WDQS4
FBA_DQS_WP5 W23 VMA_WDQS5
FBA_DQS_WP6 AB26 VMA_WDQS6
FBA_DQS_WP7 T26 VMA_WDQS7
FBA_DQS_RN0 F19 VMA_RDQS0
FBA_DQS_RN1 C14 VMA_RDQS1
FBA_DQS_RN2 A16 VMA_RDQS2
FBA_DQS_RN3 A22 VMA_RDQS3
FBA_DQS_RN4 P25 VMA_RDQS4
FBA_DQS_RN5 W22 VMA_RDQS5
FBA_DQS_RN6 AB27 VMA_RDQS6
FBA_DQS_RN7 T27 VMA_RDQS7
FB_VREF_PROBE D23 TP60
INT
tga585-nvidia-n15p-gs0-a-a2
COMMON
VMA_DQ[63:0] VMA_DQ[63:0] [20,21]
VMA_DM[7:0] [20,21]
VMA_WDQS[7:0] [20,21]
VMA_RDQS[7:0] [20,21]
FBVDDQ + FBVDD = 3.116A
+1.5V_GFX
U39D
12/14 FBVDDQ
C380 EV@0.1U/10V_4
C367 EV@0.1U/10V_4
C358 2 EV@1U/10V_6
C378 2 EV@1U/10V_6
C377 EV@4.7u/10V_6
C382 EV@4.7u/10V_6
C368 EV@10U/6.3V_6
C369 EV@22U/6.3V_8
B26 FBVDDQ
C25 FBVDDQ
E23 FBVDDQ
E26 FBVDDQ
F14 FBVDDQ
F21 FBVDDQ
G13 FBVDDQ
G14 FBVDDQ
G15 FBVDDQ
G16 FBVDDQ
G18 FBVDDQ
G19 FBVDDQ
G20 FBVDDQ
G21 FBVDDQ
H24 FBVDDQ
H26 FBVDDQ
J21 FBVDDQ
K21 FBVDDQ
L22 FBVDDQ
L24 FBVDDQ
L26 FBVDDQ
M21 FBVDDQ
N21 FBVDDQ
P21 FBVDDQ
T21 FBVDDQ
V21 FBVDDQ
W21 FBVDDQ
FB_CAL_PD_VDDQ D22 FB_CAL_PD_VDDQ R402 EV@40.2/F_4 +1.5V_GFX
FB_CAL_PU_GND C24 FB_CAL_PU_GND R413 EV@42.2/F_4
FB_CALTERM_GND B25 FB_CAL_TERM_GND R415 EV@51.1/F_4
tga585-nvidia-n15p-gs0-a-a2
COMMON
U39F
12/14 GND
A2 GND
AB17 GND
AB20 GND
AB24 GND
AC2 GND
AC22 GND
AC26 GND
AC5 GND
AC8 GND
AD12 GND
AD13 GND
AD6 GND
AD15 GND
AD16 GND
AD18 GND
AD19 GND
AD21 GND
AD22 GND
AE11 GND
AE14 GND
AE17 GND
AE20 GND
AB11 GND
AF1 GND
AF11 GND
AF14 GND
AF17 GND
AF20 GND
AF23 GND
AF5 GND
AF9 GND
AG2 GND
AG26 GND
AB14 GND
B1 GND
B11 GND
B14 GND
B17 GND
B20 GND
B23 GND
B27 GND
B5 GND
B8 GND
E11 GND
E14 GND
E17 GND
E2 GND
E20 GND
E22 GND
E25 GND
E5 GND
E8 GND
H2 GND
H23 GND
H25 GND
H5 GND
K11 GND
K13 GND
K15 GND
K17 GND
L10 GND
L12 GND
L14 GND
L16 GND
L19 GND
L2 GND
L23 GND
L25 GND
L5 GND
M11 GND
M13 GND
M15 GND
M17 GND
N10 GND
N12 GND
N14 GND
N16 GND
N18 GND
P11 GND
P13 GND
P15 GND
P17 GND
P2 GND
P23 GND
P26 GND
P5 GND
R10 GND
R12 GND
R14 GND
R16 GND
R18 GND
T11 GND
T13 GND
T15 GND
T17 GND
U10 GND
U12 GND
U14 GND
U16 GND
U18 GND
U2 GND
U23 GND
U26 GND
U5 GND
V11 GND
V13 GND
V15 GND
V17 GND
Y2 GND
Y23 GND
Y26 GND
Y5 GND
AA7 GND
AB7 GND
tga585-nvidia-n15p-gs0-a-a2 COMMON
+1.5V_GFX
R405 *60.4_4 F22 FBA_DEBUG0
R399 *60.4_4 J22 FBA_DEBUG1
[20,21] VMA_CLK0 D24 FBA_CLK0
[20,21] VMA_CLK0# D25 FBA_CLK0
[20,21] VMA_CLK1 N22 FBA_CLK1
[20,21] VMA_CLK1# M22 FBA_CLK1
D18 FBA_WCK01
C18 FBA_WCK01
D17 FBA_WCK23
D16 FBA_WCK23
T24 FBA_WCK45
U24 FBA_WCK45
V24 FBA_WCK67
V25 FBA_WCK67
FB_PLLAVDD = 55mA
+1.05V_GFX L22 EV@PBY160808T-300Y-N FB_PLLAVDD F16 FB_PLLAVDD
C372 EV@22U/6.3VS_6
C373 EV@0.1U/10V_4
C362 EV@0.1U/10V_4
C374 EV@0.1U/10V_4
P22 FB_PLLAVDD
H22 FB_PLLAVDD
FB_PLLAVDD GF119
FB_PLLAVDD GF117
FB_DLLAVDD = 15mA
+1.5V_GFX
EV@100/F_4 R752 FBA_CMD4 EV@100/F_4 R753
EV@100/F_4 R750 FBA_CMD5 EV@100/F_4 R751
EV@100/F_4 R435 FBA_CMD6 EV@100/F_4 R436
EV@100/F_4 R431 FBA_CMD7 EV@100/F_4 R432
EV@100/F_4 R763 FBA_CMD8 EV@100/F_4 R764
EV@100/F_4 R440 FBA_CMD9 EV@100/F_4 R441
EV@100/F_4 R462 FBA_CMD10 EV@100/F_4 R463
EV@100/F_4 R422 FBA_CMD11 EV@100/F_4 R421
EV@100/F_4 R756 FBA_CMD12 EV@100/F_4 R757
EV@100/F_4 R458 FBA_CMD13 EV@100/F_4 R459
EV@100/F_4 R759 FBA_CMD14 EV@100/F_4 R760
EV@100/F_4 R420 FBA_CMD15 EV@100/F_4 R419
EV@100/F_4 R465 FBA_CMD21 EV@100/F_4 R464
EV@100/F_4 R451 FBA_CMD22 EV@100/F_4 R450
EV@100/F_4 R468 FBA_CMD23 EV@100/F_4 R467
EV@100/F_4 R442 FBA_CMD24 EV@100/F_4 R443
EV@100/F_4 R427 FBA_CMD25 EV@100/F_4 R428
EV@100/F_4 R457 FBA_CMD26 EV@100/F_4 R456
EV@100/F_4 R452 FBA_CMD27 EV@100/F_4 R453
EV@100/F_4 R426 FBA_CMD28 EV@100/F_4 R425
EV@100/F_4 R430 FBA_CMD29 EV@100/F_4 R429
EV@100/F_4 R446 FBA_CMD30 EV@100/F_4 R447
For support GC6 2.0
+3V
C267 GT@0.1U/10V_4
[19,31] EC_FB_CLAMP
[10,19] GC6_FB_EN
[38] GPU_PWR_GD
R358 *0_4
R357 GT@0_4
FBVDDQ_EN [39]
U20 GT@NL17SZ32DFT2G
R362 EV@100K/F_4
R359 GM@0_4
Quanta Computer Inc.
PROJECT : ZRT/ZRTA
Size
Document Number
N16S-GT (MEMORY/GND)
Rev 3A
Date: Wednesday, February 11, 2015
Sheet 17 of 44


IFPAB
IFPC
IFPD
IFPE
IFPF
3V MAIN POWER
PLLVDD = 38mA
SP_PLLVDD = 17mA
VID_PLLVDD = 41mA
DB-->SI change 10/25
Use G-CLK
DB-->SI change 10/25
Use G-CLK
+1.05V_GFX and GPU core power EN
N15V stuff not support GC6.
Quanta Computer Inc.
PROJECT : ZRT/ZRTA
N16S-GT (DISPLAY)
Wednesday, February 11, 2015



N16S-GS/N16V-GM Straping table

ROM_SI N16S	
2G Hynix 128Mx16	-->34.8K PD
2G Micron 128Mx16	-->45.3K PD
2G Samsumg 128Mx16	-->4.99K PU
4G Hynix 256Mx16	-->4.99K PD
4G Micron 256Mx16	-->10K PD
4G Samsumg 256Mx16	-->15K PD

ROM_SI N16V	
2G Hynix 128Mx16	-->20K PD
2G Micron 128Mx16	-->30.1K PD
2G Samsumg 128Mx16	-->34.8K PD
4G Micron 256Mx16	-->10K PD
4G Hynix 256Mx16	-->15K PD
4G Samsumg 256Mx16	-->24.9K PD

Resistor P/N

4.99K--->	CS24992FB26
10K --->	CS31002FB26
15K --->	CS31502FB24
20K --->	CS32002FB29
24.9K --->	CS32492FB16
30.1K --->	CS33012FB18
34.8K--->	CS33482FB22
45.3K --->	CS34532FB18 GM
49.9K --->	CS34992FB10 GT

ROM_SO	ROM_SCLK	STRAP0
N16S-GT --> 4.99K PD	N16S-GT --> 4.99K PD	N16S-GT --> 49.9K PU
N16V-GM --> 4.99K PU	N16V-GM --> 4.99K PU	N16V-GM --> 45.3K PU

N16V-GM strap0-3 table

STRAP0	= Stuff 45.3k pull up. (EDID Panel)
STRAP1	= Stuff 4.99k pull down.(Gen3 support)
STRAP2	= Stuff 10k pull up.(DID 0x1299)
STRAP3	= Stuff 4.99k pull down.(No display out)
STRAP4	= Stuff 45.3k pull down. (Gen3/max speed)

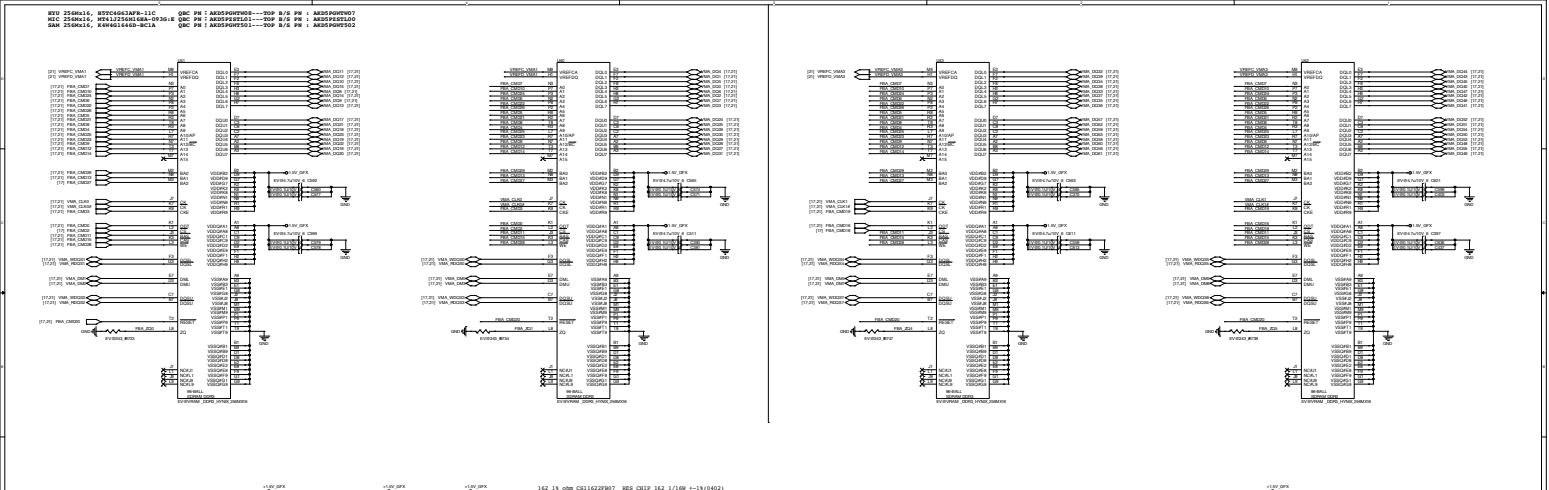
Logical Strap Bit Mapping

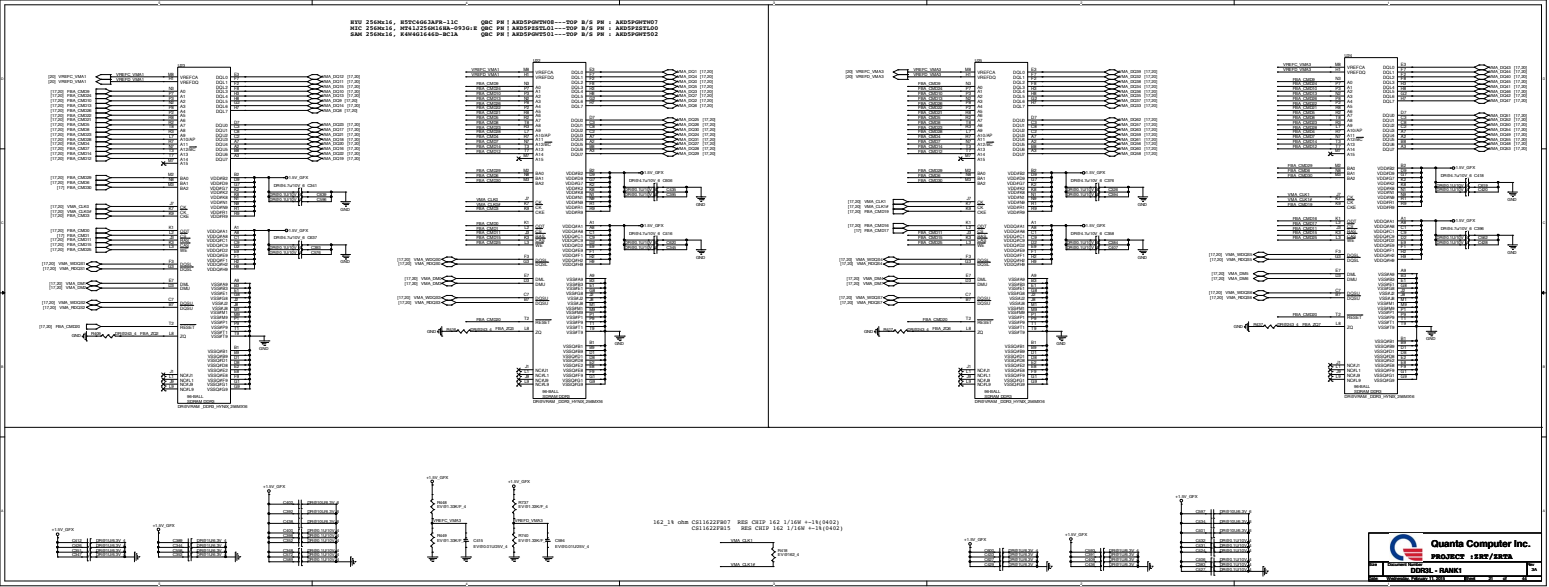
	PU-VDD	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

Quanta Computer Inc.

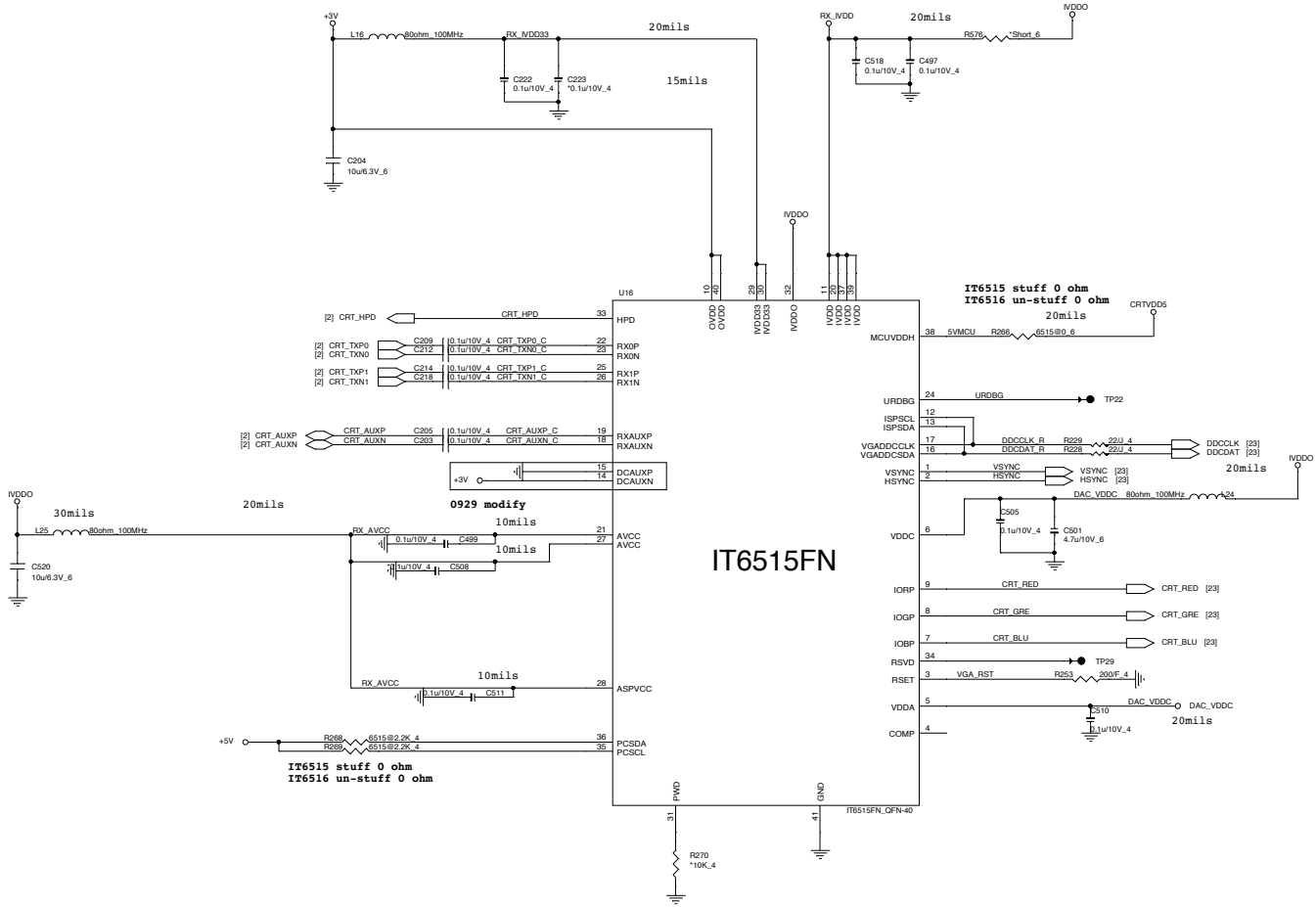
PROJECT : ZRT/ZRTA

Size	Document Number	Rev
	N16S-GT (GPIO/STRAPS)	3A
Date: Wednesday, February 11, 2015	Sheet 19 of 44	


BYU 256Kx16, 85TC4G63AFB-11C QBC PN : AKD5PGHTW08---TOP B/S PN : AKD5PGHTW07
HIC 256Kx16, MT41J256M16HA-093G:E QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
SAM 256Kx16, K4W4G1646D-BCLA QBC PN : AKD5PGHWT01---TOP B/S PN : AKD5PGHWT02
U61
U62
U63
U64
DDR3_DIMM_204PIN_VTYPE_SMD0930
162_1% ohm CS11622FB07 RES CHIP 162 1/16W +-1%(0402)
CS11622FB15 RES CHIP 162 1/16W +-1%(0402)
FOR EMI Request
Quanta Computer Inc.
PROJECT :1ZR/1ZRTA
DDR3L - RANK0


MTU 256Mx16, MT5C6463AFB-11C QBC PN : ARDSPGWTN08---TOP B/S PN : ARDSPGWTN07
NIC 256Mx16, M5412256G16BA-0T3G:E QBC PN : ARDSPSETL01---TOP B/S PN : ARDSPSETL02
ESM 256Mx16, K4H561646B-BCLA QBC PN : ARDSPGWTS01---TOP B/S PN : ARDSPGWTS02
162_1% ohm CS1162ZP807 RSS CHIP 162 1/16W +-1%(0402)
CS1162ZP915 RSS CHIP 162 1/16W +-1%(0402)
Quanta Computer Inc.
PROJECT :1ZE/1ZETA
DDRSL - RANK1

DP TO VGA



[2,5,7,8,9,10,11,13,14,15,16,17,18,23,24,25,26,27,28,29,30,31,33,34,35,36,37,38,39] +3V
[23,24,26,27,29,33,37] +5V

Quanta Computer Inc.		
PROJECT : ZRT/ZRTA		
Size	Document Number: DP to VGA iT6165	Rev: 3A
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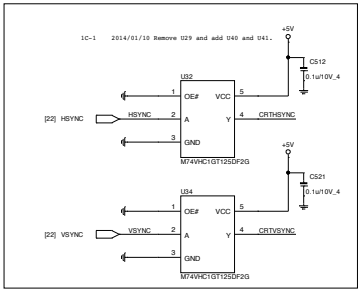
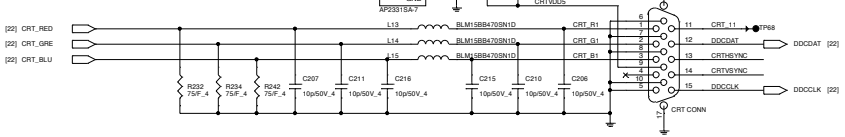
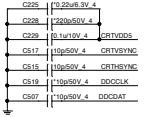
CRT



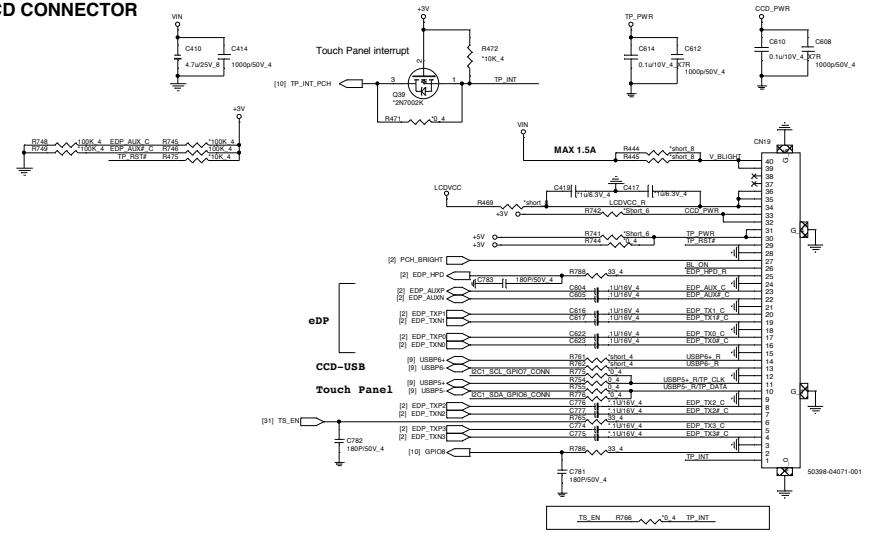




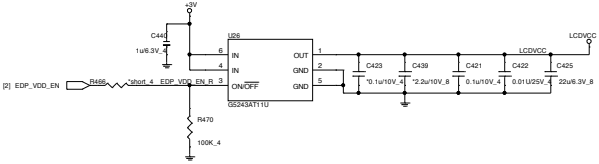
Power trace tracking

[2,5,7,8,9,10,11,13,14,15,16,17,18,22,24,25,26,27,28,29,30,31,33,34,35,36,37,38,39] +3V
[22,24,26,27,29,33,37] +5V
[7,8,10,11,13,25,26,27,28,29,31,32,33,37,38,39] +3VPCU
[27,29,32,33,34,35,36,37,38,39] VIN

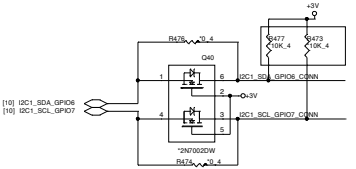
LCD CONNECTOR

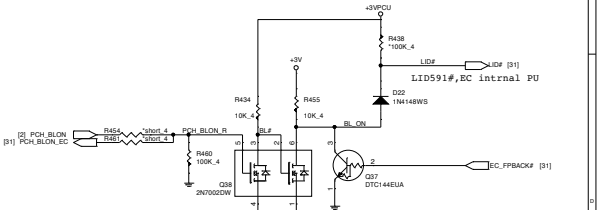


LCD Power

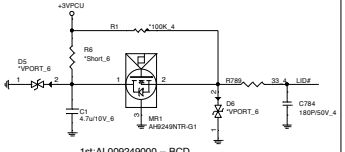


Touch screen level shift I2C(reserve)





Hall Sensor (HSR)



1st:AL009249000 -- BCD
2nd:AL009132001 -- ANC

Quanta Computer Inc.			
PROJECT : ZRT/ZRTA			
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	CRT/LVDS/CAMERA/LID		1A
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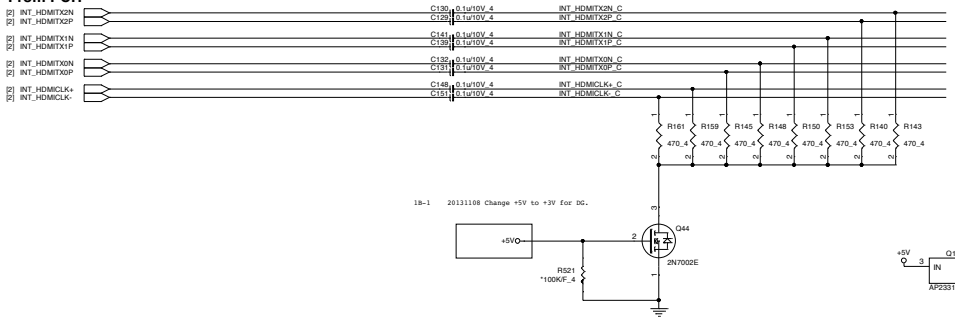
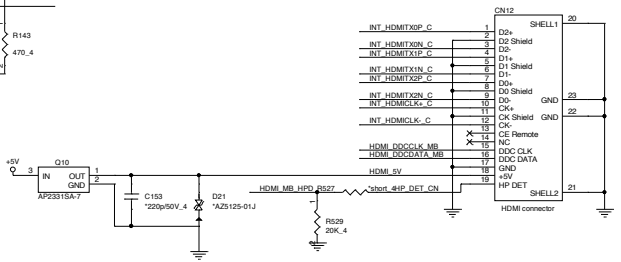
HDMI

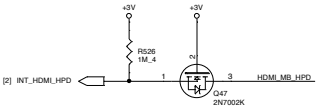
From PCH



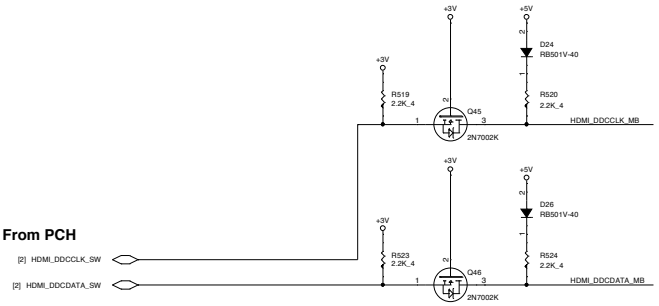
HDMI connector



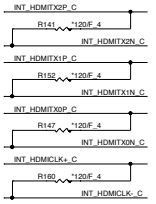
HDMI-detect



I2C



EMI



Power trace tracking

[2,5,7,8,9,10,11,13,14,15,16,17,18,22,23,25,26,27,28,29,30,31,33,34,35,36,37,38,39] +3V
[22,23,26,27,29,33,37] +5V

Quanta Computer Inc.
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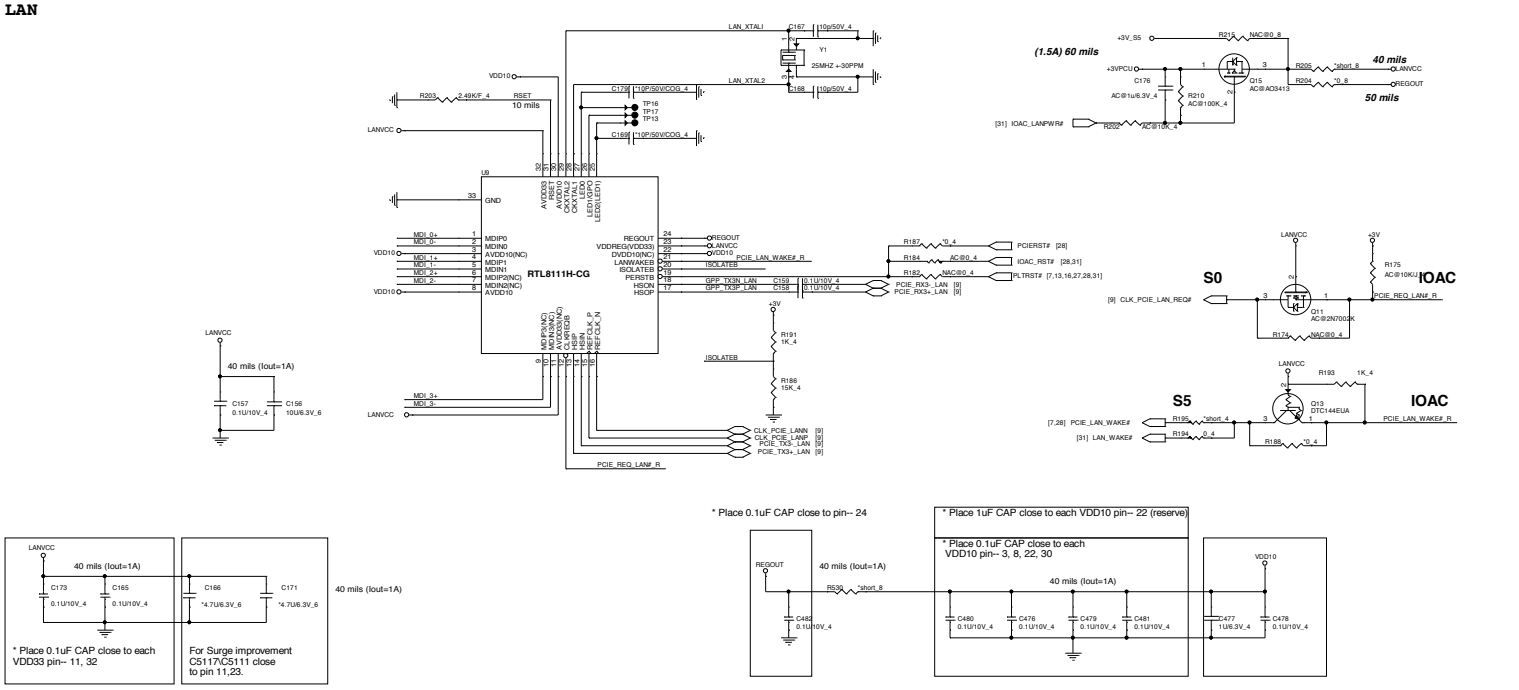
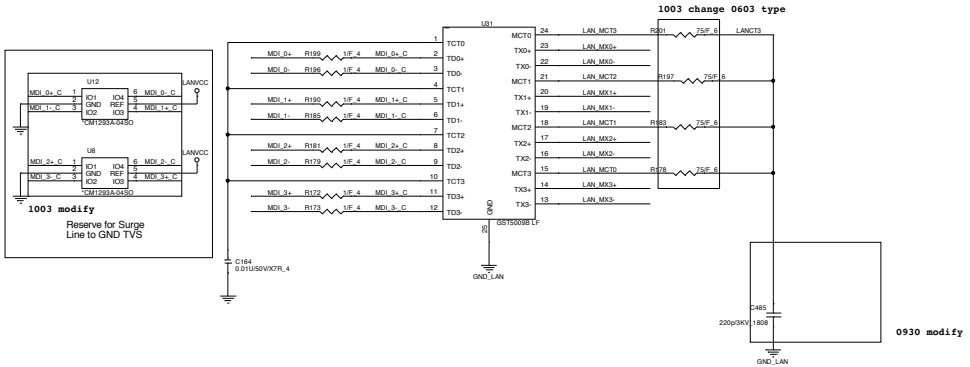
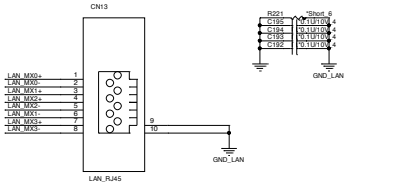
LAN



Tramsformer



RJ45 Connector



Power trace tracking

[2,5,7,8,9,10,11,13,14,15,16,17,18,22,23,24,26,27,28,29,30,31,33,34,35,36,37,38,39] +3V
[5,7,8,9,10,11,13,27,29,31,33,36,38] +3V_S5
[7,8,10,11,13,23,26,27,28,29,31,32,33,37,38,39] +3VPCU

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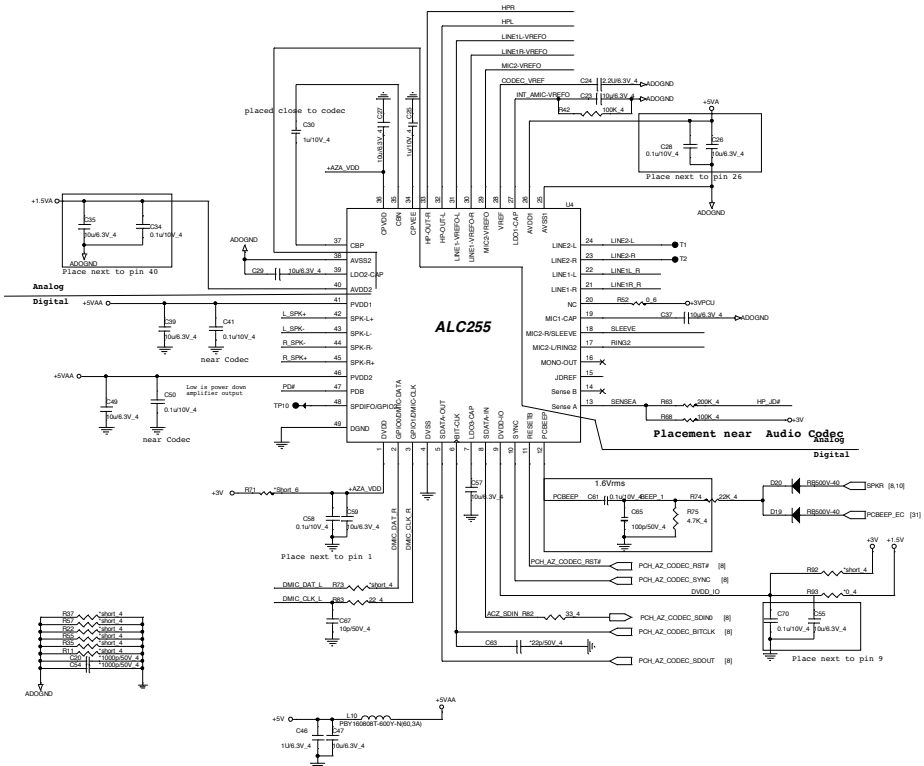
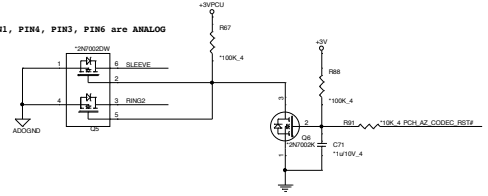
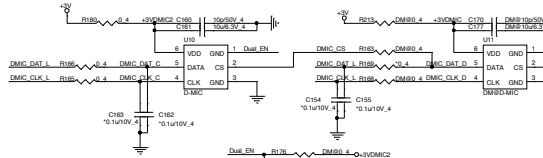
Codec(ADO)



Grounding circuit(ADO)

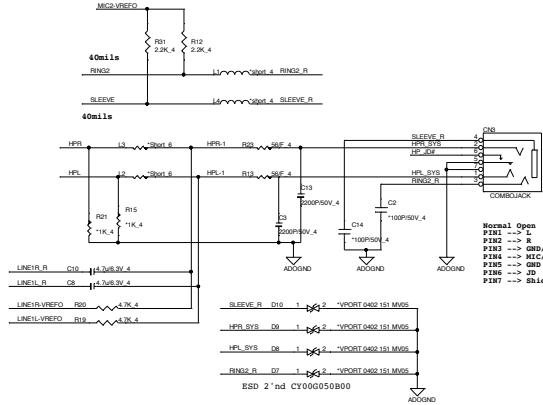


D-Mic

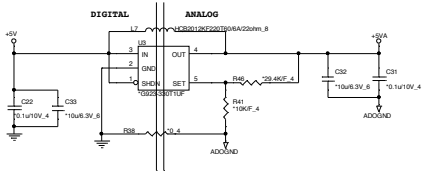


1.Single DMIC
KMM47237626-06DT (AL472376000) (MAIN)
SPM0437HD4H (AL000437000)
2.Dual DMIC
KMM47237622-10DT(AL472376001) (MAIN)
NSM0410DT (W/ Fortemedia algorithm)
Main MIC CS need connect to second MIC DATA

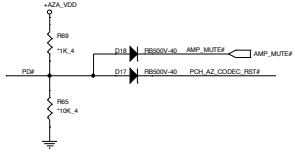
Universal Audio Jack



Codec PWR 5V(ADO)

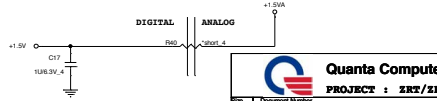


Mute(ADO)



Internal Speaker

Codec PWR 3V/1.5V(ADO)



Quanta Computer Inc.
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	ALC283/HP/SPK	3B
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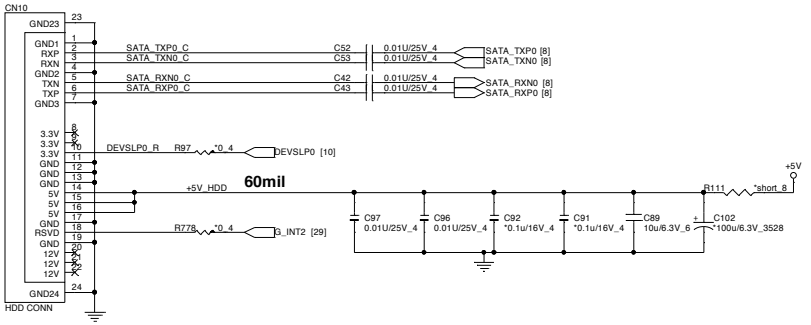
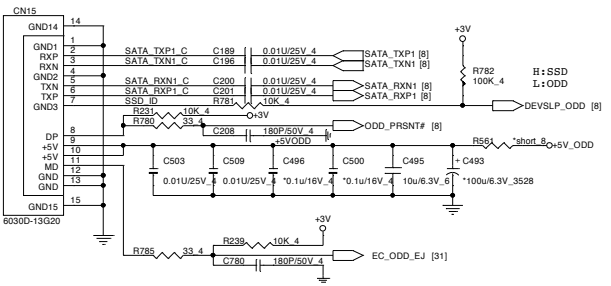
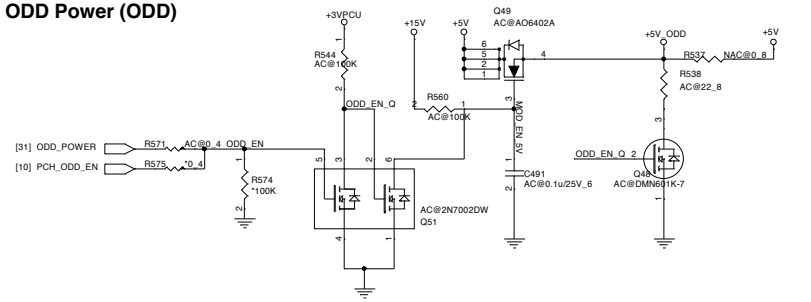
2.5" SATA HDD (HDD)



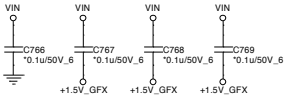
SATA ODD Connector(ODD)



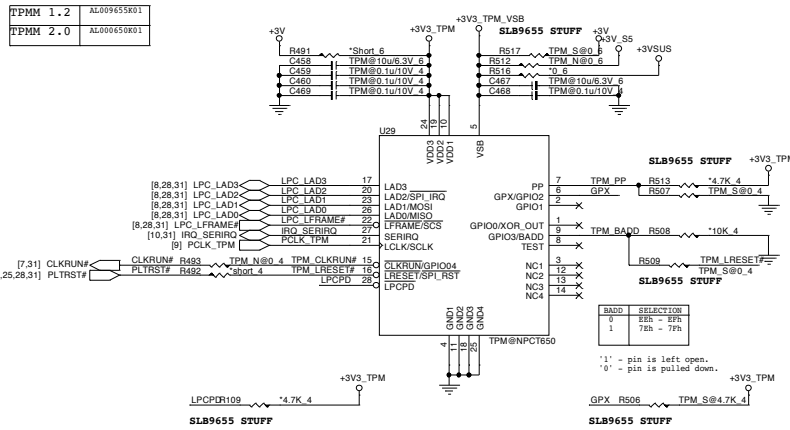
ODD Power (ODD)



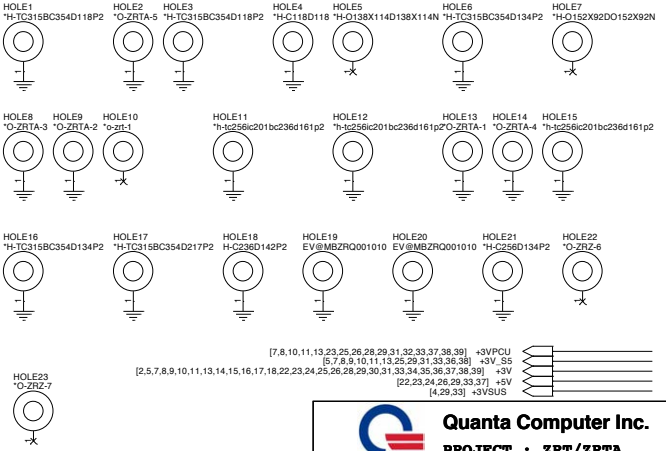
EMI



TPM NPCT650 (TPM)



HOLE / MOUNTING



[7,8,10,11,13,23,25,26,28,29,31,32,33,37,38,39] +3VPCU
[5,7,8,9,10,11,13,25,29,31,33,36,38] +3V_S5
[2,5,7,8,9,10,11,13,14,15,16,17,18,22,23,24,25,26,28,29,30,31,33,34,35,36,37,38,39] +3V
[22,23,24,26,29,33,37] +5V
[4,29,33] +3VSUS

Quanta Computer Inc.

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	HDD/ODD/TPM NPCT650	1A
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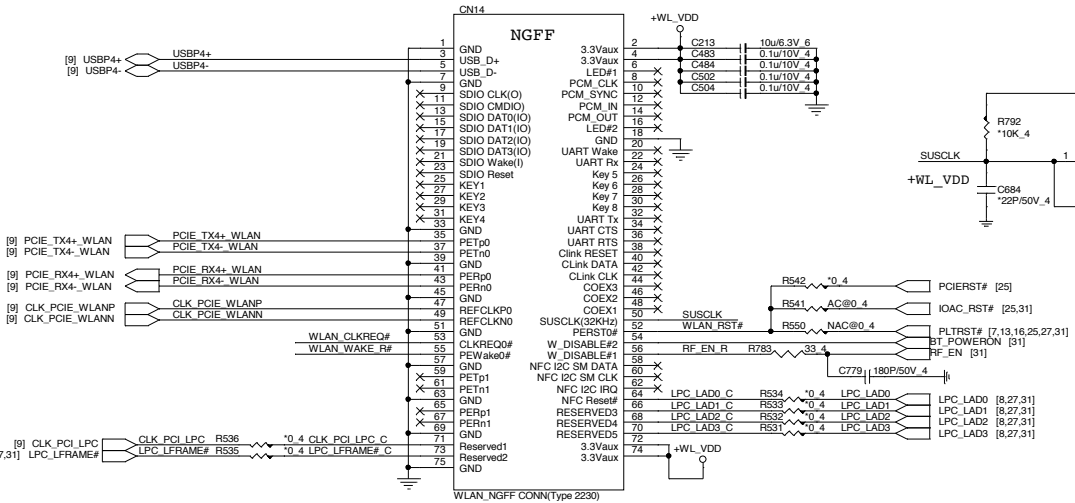
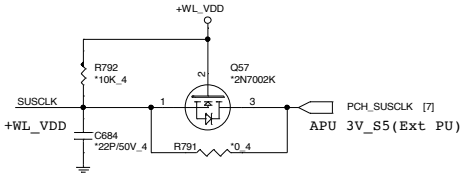
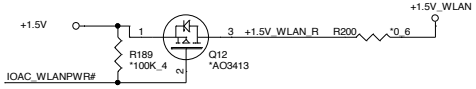
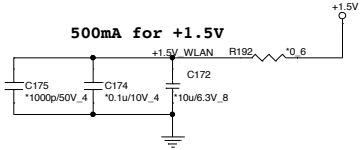
NGFF WiFi & BT (NGF)

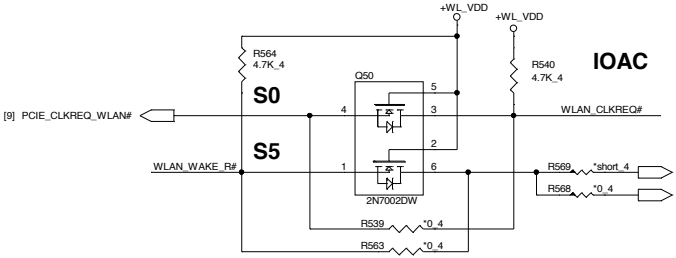
[7,8,10,11,13,23,25,26,27,29,31,32,33,37,38,39] +3VPCU
[11,26,37] +1.5V
[2,5,7,8,9,10,11,13,14,15,16,17,18,22,23,24,25,26,27,29,30,31,33,34,35,36,37,38,39] +3V

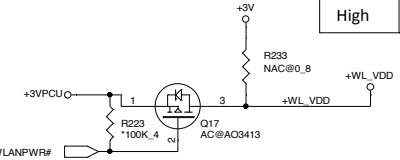












Low	Mini card +3V power enable
High	Mini card +3V power disable

High	Mini card +3V power disable

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	Mini-Card/WL/3G/SIM	1A
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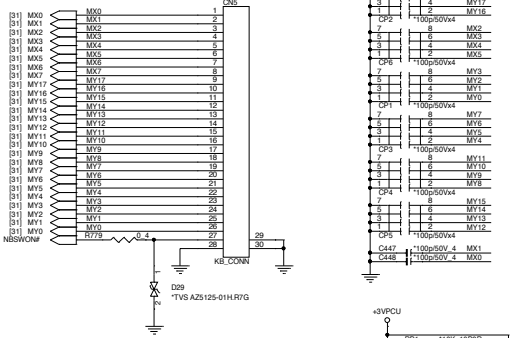
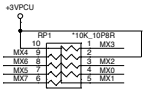
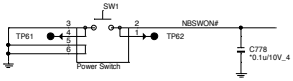
K/B (KBC)

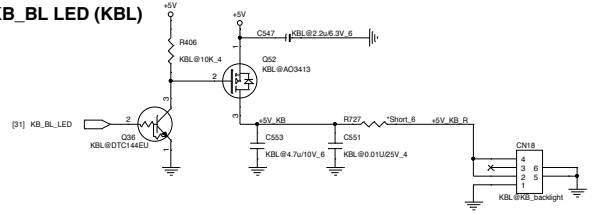




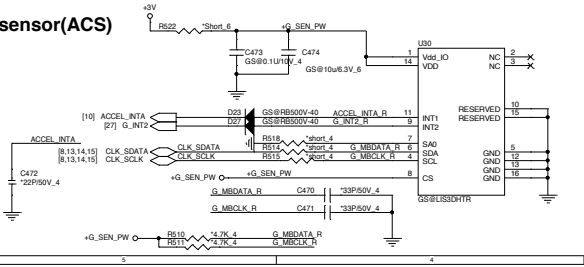
For test only



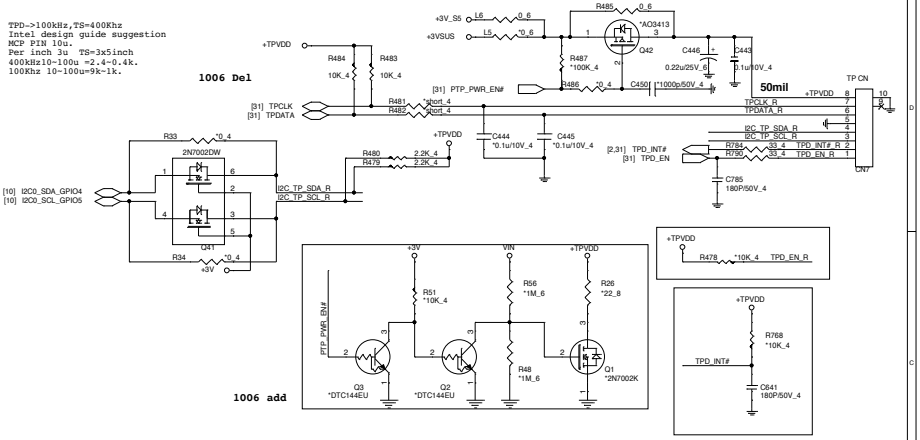
KB_BL LED (KBL)



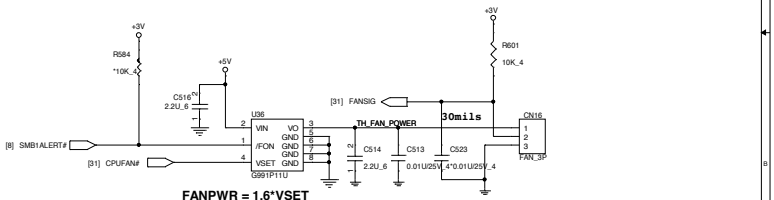
G-sensor(ACS)



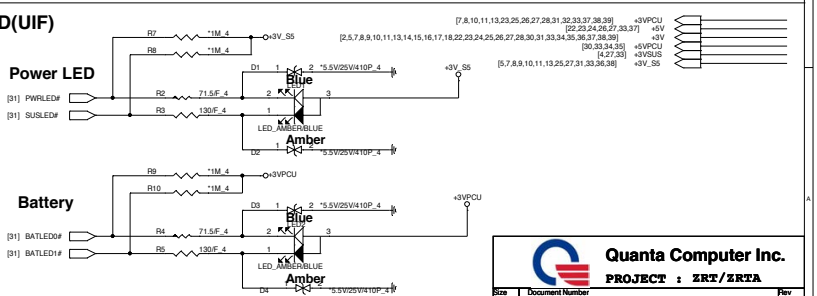
TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay)



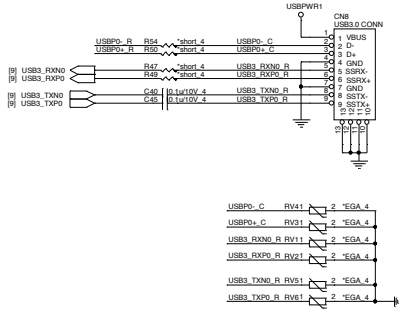
CPU FAN (THM)



POWER LED(UIF)



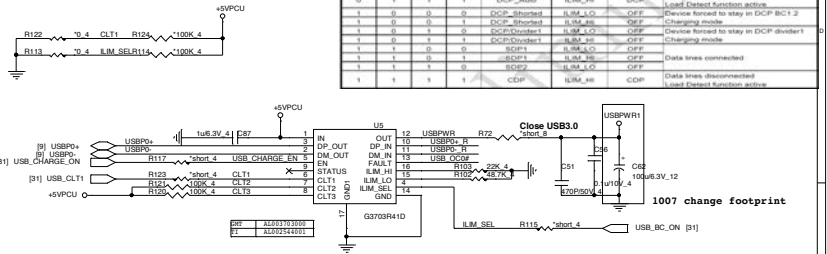
USB 3.0 Connector(UB3)



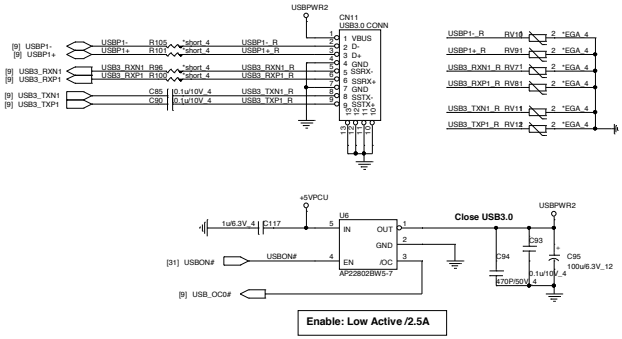
USB Charger for USB3.0 Port0 (UBC)

Table 2. Truth Table

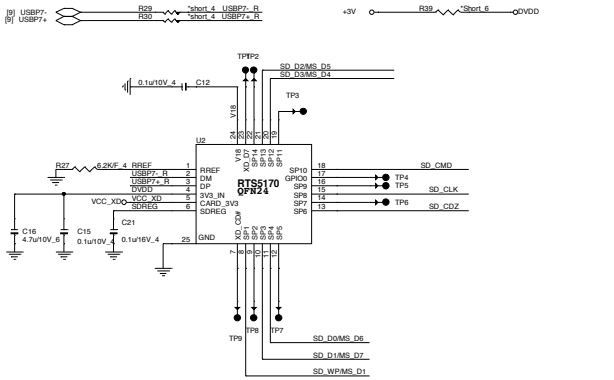
CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Status Output	Notice
0	0	0	0	Discharge	NA	OFF	
0	0	0	1	Discharge	NA	OFF	OUT held low
0	0	1	0	DCP_Auto	ILIM_HI	OFF	Data lines disconnected
0	0	1	1	DCP_Auto	ILIM_HI	DCP	Data lines disconnected Load Detect function active
0	1	0	0	SDP1	ILIM_LO	OFF	Data lines connected
0	1	0	1	SDP1	ILIM_HI	OFF	
0	1	1	0	DCP_Auto	ILIM_LO	OFF	Data lines disconnected
0	1	1	1	DCP_Auto	ILIM_HI	DCP	Data lines disconnected Load Detect function active
1	0	0	0	DCP_Shorted	ILIM_LO	OFF	Device forced to stay in DCP BC1.2
1	0	0	1	DCP_Shorted	ILIM_HI	OFF	Charging mode
1	0	1	0	DCP/Divider1	ILIM_LO	OFF	Device forced to stay in DCP divider1
1	0	1	1	DCP/Divider1	ILIM_HI	OFF	Charging mode
1	1	0	0	SDP1	ILIM_LO	OFF	
1	1	0	1	SDP1	ILIM_HI	OFF	Data lines connected
1	1	1	0	SDP2	ILIM_LO	OFF	
1	1	1	1	CDP	ILIM_HI	CDP	Data lines disconnected Load Detect function active



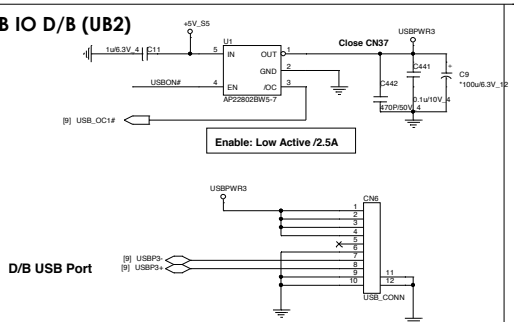
USB 3.0 Connector(UB3)



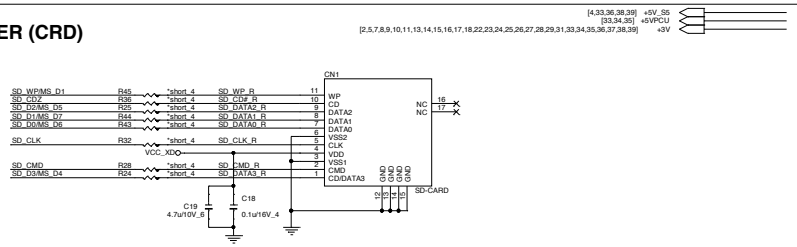
Card Reader (CRD)



USB IO D/B (UB2)



SD/MMC CARD READER (CRD)



Quanta Computer Inc.
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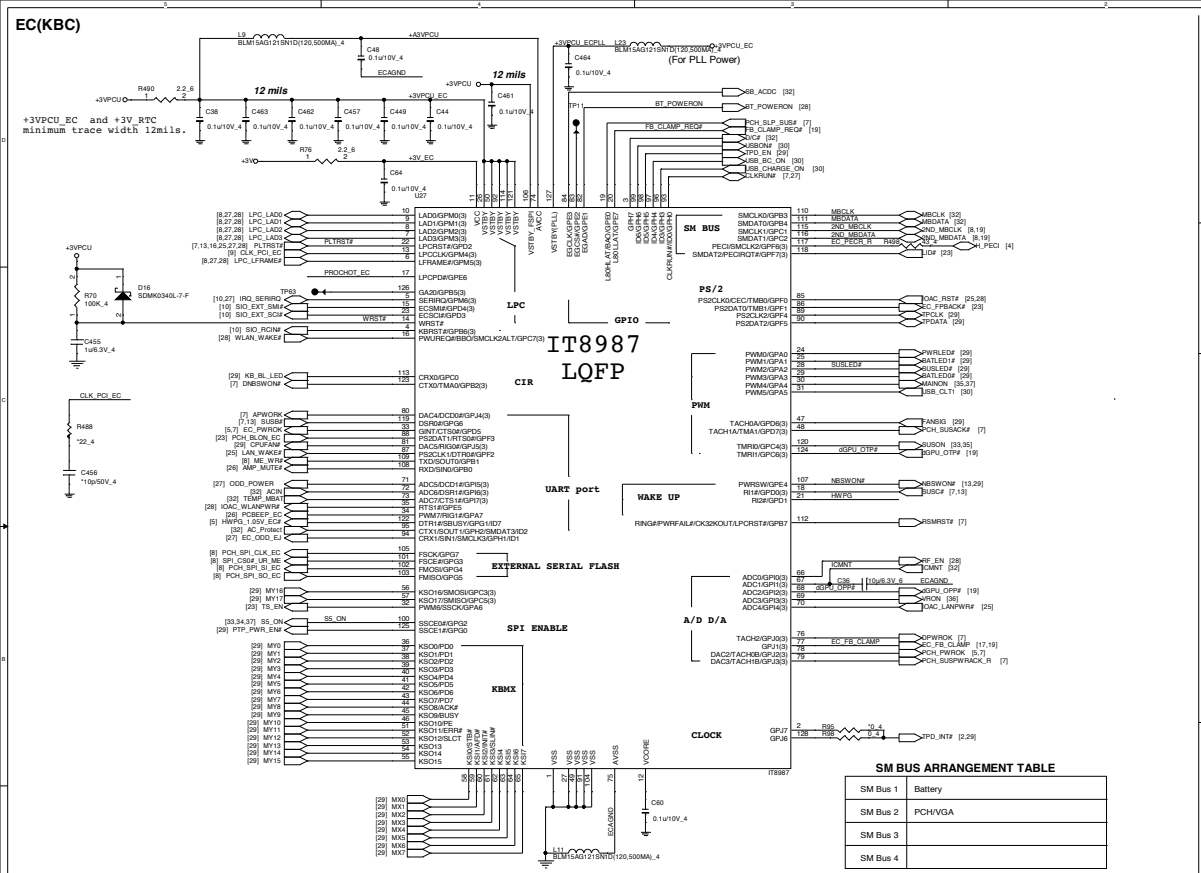
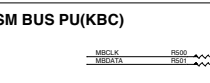
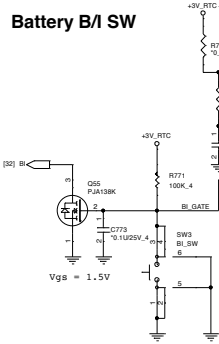
EC(KBC)



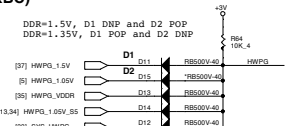
SM BUS PU(KBC)



Battery B/I SW



HWPG(KBC)



SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH/VGA
SM Bus 3	
SM Bus 4	

[7,8,10,11,13,23,25,26,27,28,29,32,33,37,38,39] +3VPCU
[16,18,19,39] +3V_GFX
[2,5,7,8,9,10,11,13,14,15,16,17,18,22,23,24,25,26,27,28,29,30,33,34,35,36,37,38,39] +3V
[5,7,8,9,10,11,13,25,27,29,33,36,38] +3V_S5

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Size: Document Number: KBC IT8587 Rev: 3A
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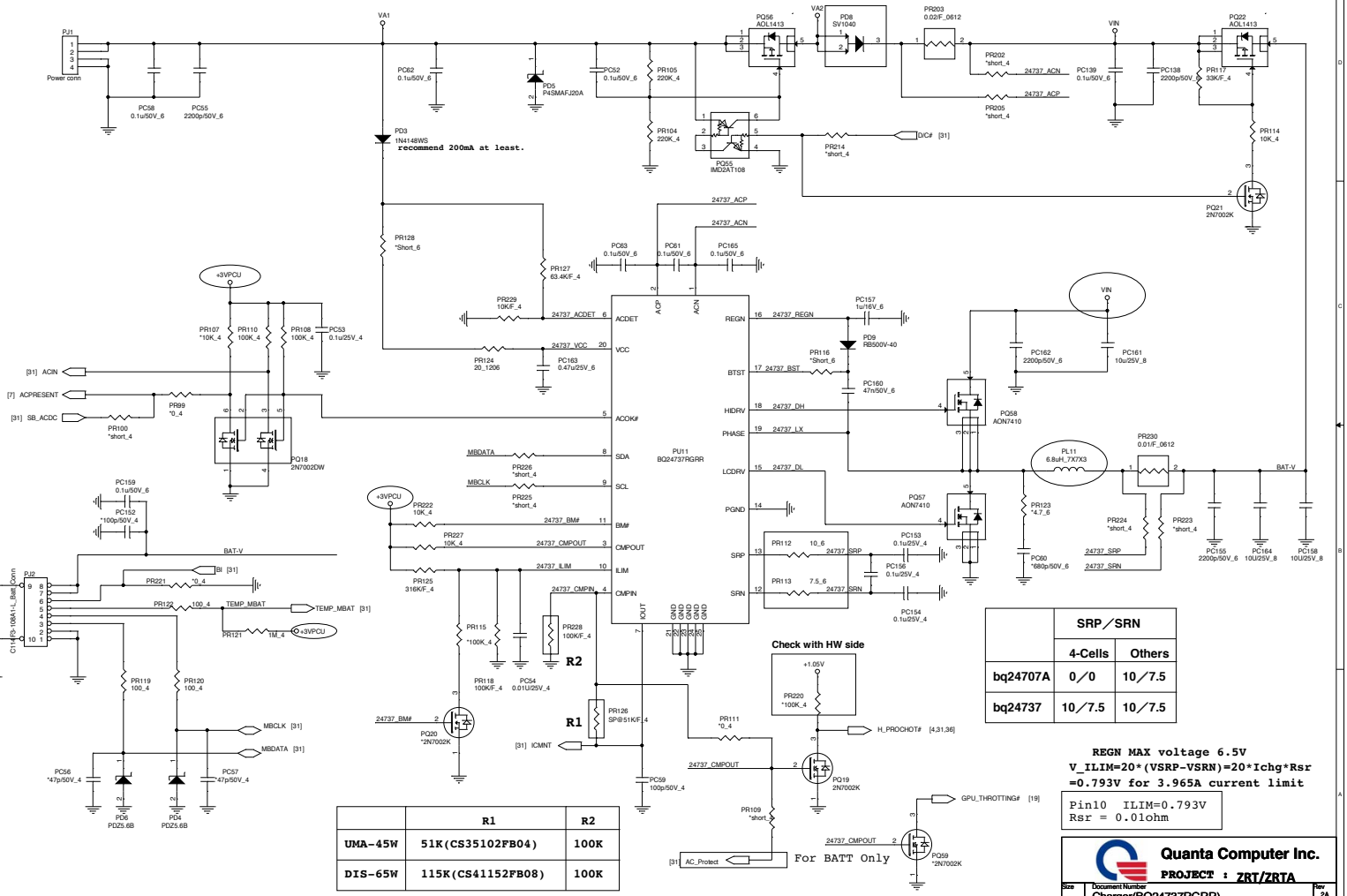

	R1	R2
UMA-45W	51K(CS35102FB04)	100K
DIS-65W	115K(CS41152FB08)	100K

	SRP／SRN	
	4-Cells	Others
bq24707A	0／0	10／7.5
bq24737	10／7.5	10／7.5

REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit

Pin10 ILIM=0.793V
Rsr = 0.01ohm

Quanta Computer Inc.
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Size	Document Number	Rev
	Charger(BQ24737RGRR)	2A
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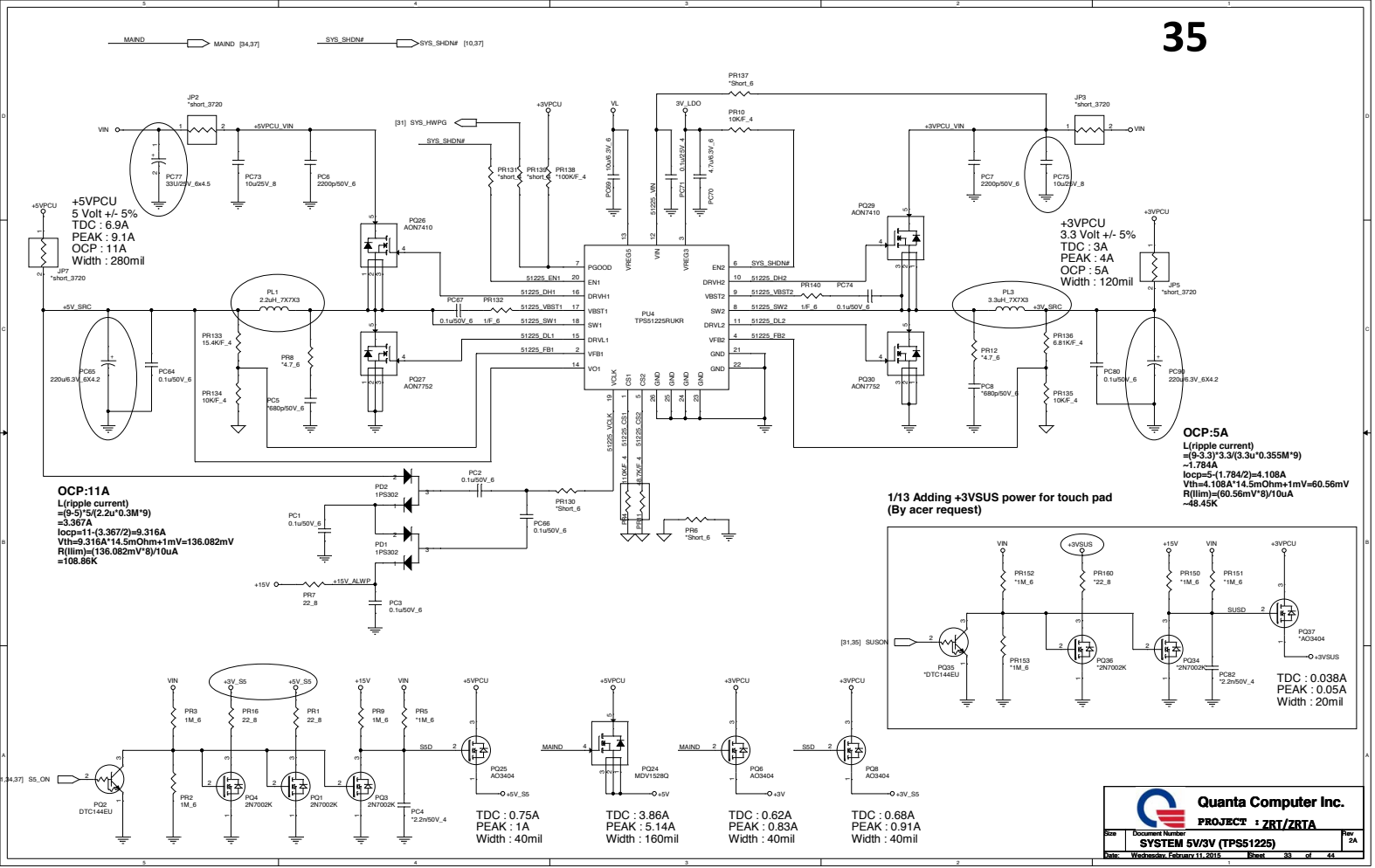
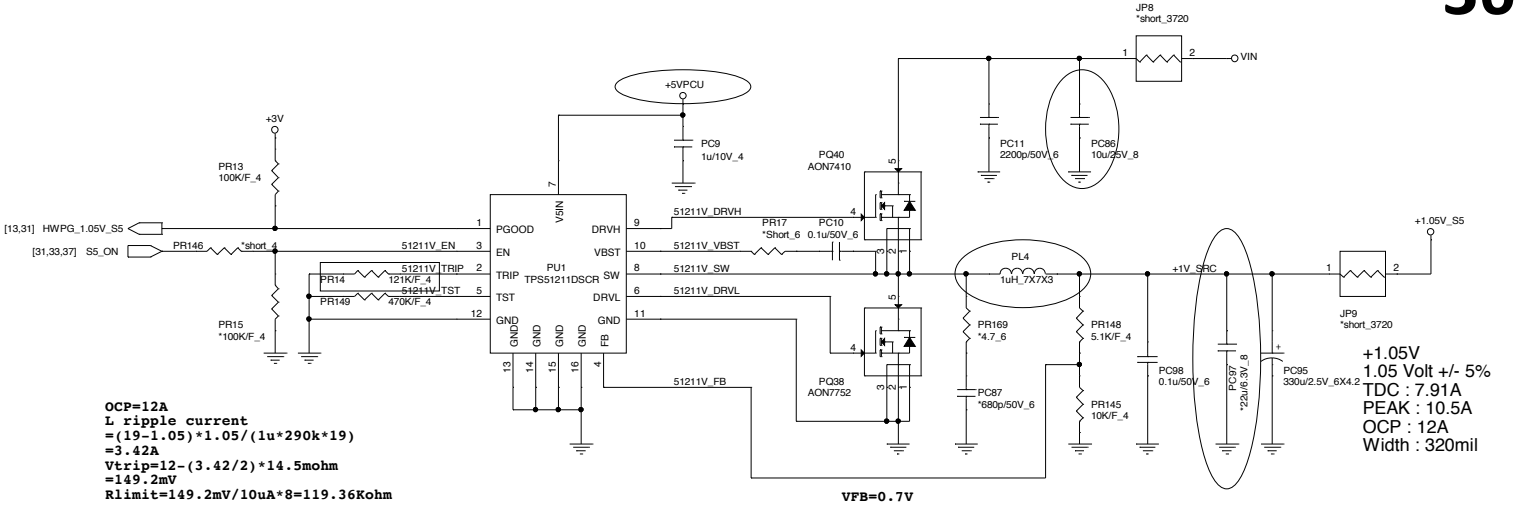
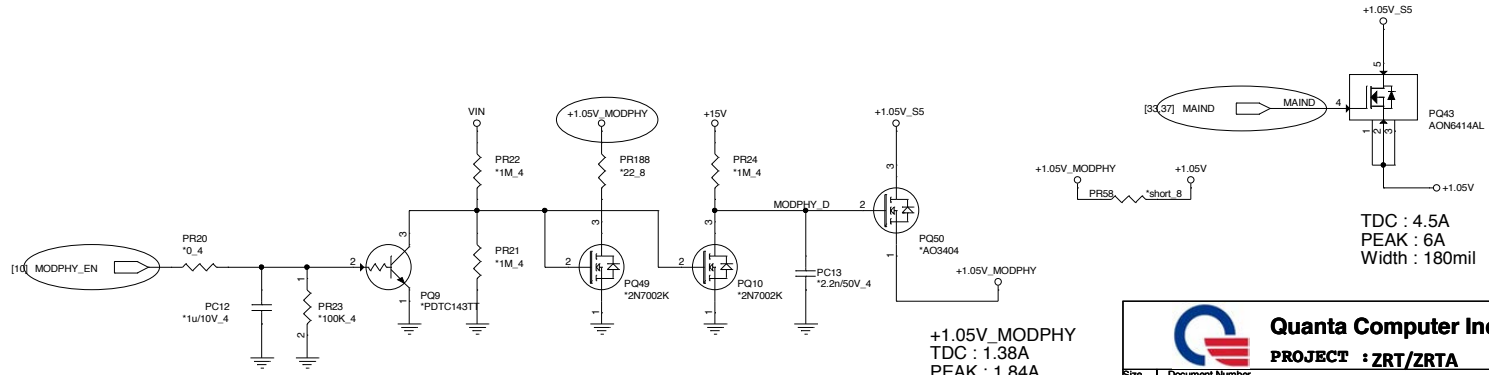

MAIND
MAIND [34,37]
SYS_SHDN#
SYS_SHDN# [10,37]
+5VPCU
5 Volt +/- 5%
TDC : 6.9A
PEAK : 9.1A
OCP : 11A
Width : 280mil
+3VPCU
3.3 Volt +/- 5%
TDC : 3A
PEAK : 4A
OCP : 5A
Width : 120mil
OCP:11A
L(ripple current)
=(9-5)*5/(2.2u*0.3M*9)
=3.367A
Iocp=11-(3.367/2)=9.316A
Vth=9.316A*14.5mOhm+1mV=136.082mV
R(Ilim)=(136.082mV*8)/10uA
=108.86K
OCP:5A
L(ripple current)
=(9-3.3)*3.3/(3.3u*0.355M*9)
~1.784A
Iocp=5-(1.784/2)=4.108A
Vth=4.108A*14.5mOhm+1mV=60.56mV
R(Ilim)=(60.56mV*8)/10uA
~48.45K
1/13 Adding +3VSUS power for touch pad
(By acer request)
TDC : 0.038A
PEAK : 0.05A
Width : 20mil
TDC : 0.75A
PEAK : 1A
Width : 40mil
TDC : 3.86A
PEAK : 5.14A
Width : 160mil
TDC : 0.62A
PEAK : 0.83A
Width : 40mil
TDC : 0.68A
PEAK : 0.91A
Width : 40mil
PROJECT : ZRT/ZRTA
SYSTEM 5V/3V (TPS51225)
Wednesday, February 11, 2015
Sheet 33 of 44





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PROJECT : ZRT/ZRTA		
Size	Document Number: +1.05V_S5 (TPS51211)	Rev: 2A
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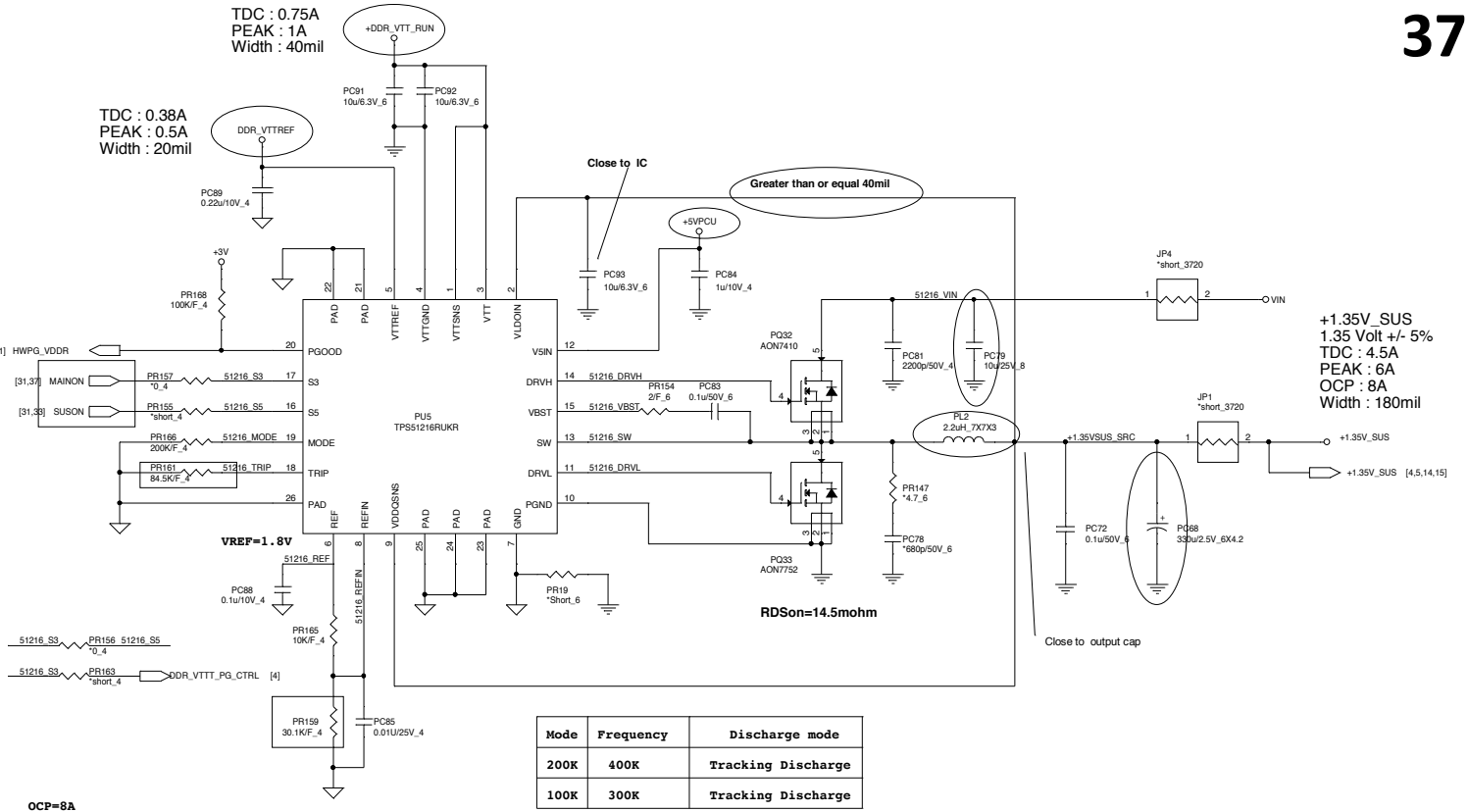


+1.35V_SUS
1.35 Volt +/- 5%
TDC : 4.5A
PEAK : 6A
OCP : 8A
Width : 180mil

Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

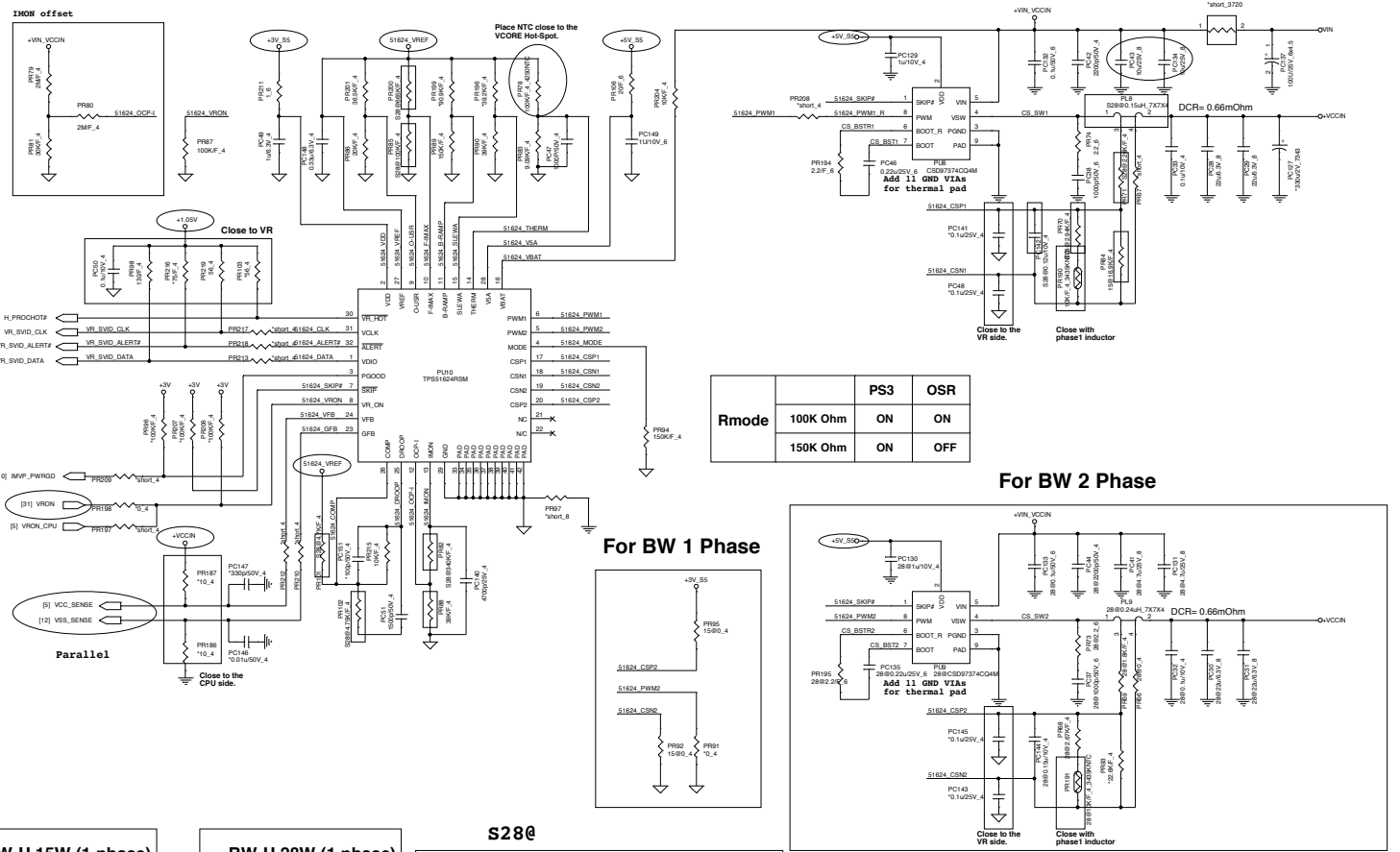
	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

OCP=8A
L ripple current
=(19-1.35)*1.35/(2.2u*400k*19)
=1.425A
Vtrip=8-(1.425/2)*14.5mohm
=105.668mV
Rlimit=105.668mV/10uA*8=84.53Kohm

DDR=1.35V
PR84=10K/F_4
PR86=30.1K/F_4

Quanta Computer Inc.
PROJECT : ZRT/ZRTA

Size	Document Number	Rev
	DDR 1.35V(TPS51216)	2A
Date: Wednesday, February 11, 2015	Sheet 35 of 44	



Rmode		PS3	OSR
	100K Ohm	ON	ON
	150K Ohm	ON	OFF

BW-U 15W (1 phase)

Icc TDC PL2：14A

Icc Max：32A

OCP：37A

Fsw：1.2MHz

VCORE L/L：

R_DC_LL：- 2.0mV/A

R_AC_LL：- 7.0mV/A

BW-U 28W (1 phase)

Icc TDC PL2：19A

Icc Max：40A

OCP：47A

Fsw：800KHz

VCORE L/L：

R_DC_LL：- 2.0mV/A

R_AC_LL：- 7.0mV/A

S28@

BW-U 28W 2 phase			
Location	Value	Location	Value
PL8	CV+24P0MZ00	PR85	CS35622FB10
PR71	CS21822FB14	PR101	CS22372FB11
PR82	CS41502FB18	PR102	CS31002FB26
PR70	CS22672FB12	PR200	CS42942FB13
PC142	CH4152K9B02		
Block 1.	Stuff		

PL9 0.24uH_7X7X4

PR84、PR93 *22.6K/F_4

PR92、PR95 *0_4

PC143、PC145 *0.1u/25V_4

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PROJECT : ZRT/ZRTA			
Size	Document Number		Rev
	+VCCIN(TPS51624)		2A
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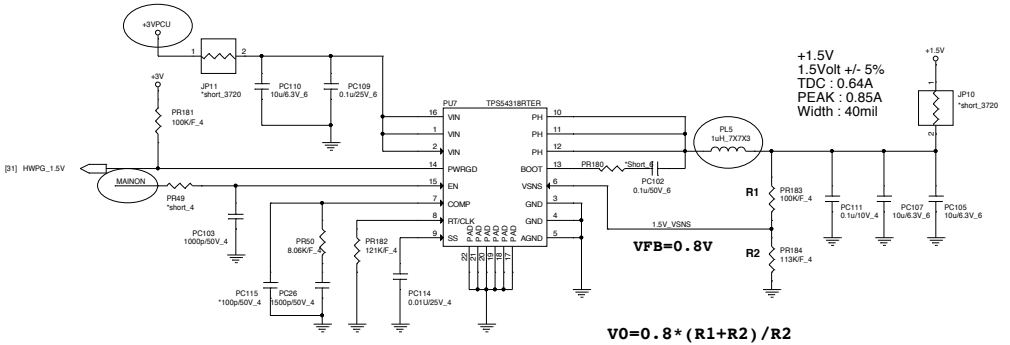
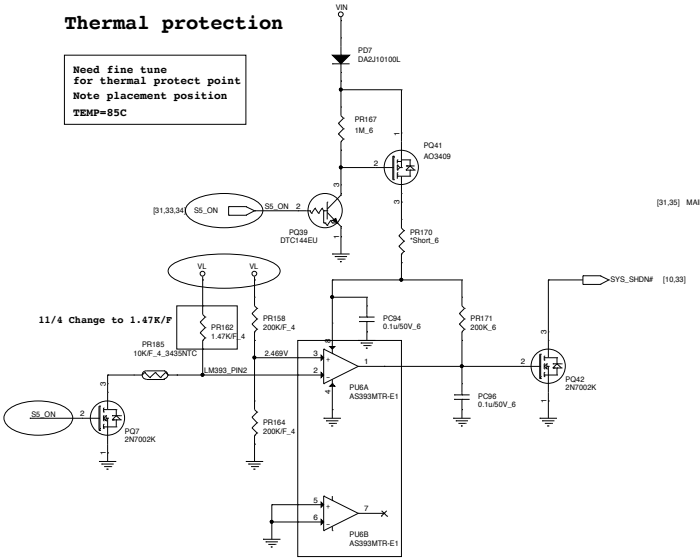


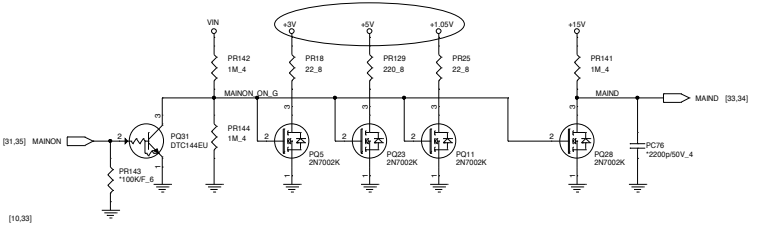
V0=0.8*(R1+R2)/R2

Thermal protection

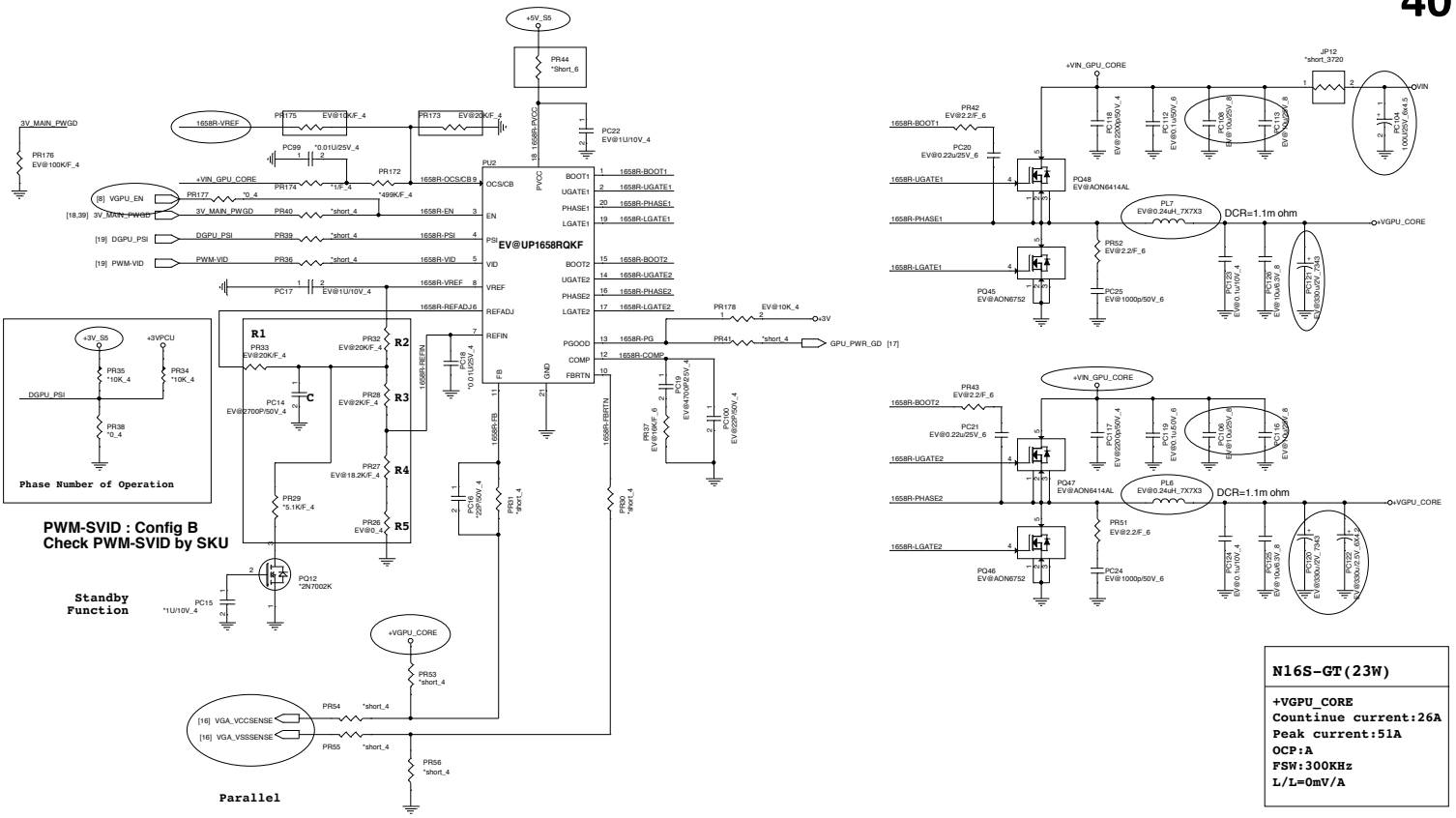
Need fine tune
for thermal protect point
Note placement position

TEMP=85C





For EC control thermal protection (output 3.3V)



N16S-GT(23W)

+VGPU_CORE
Countinue current:26A
Peak current:51A
OCP:A
FSW:300KHz
L/L=0mV/A

Quanta Computer Inc.
PROJECT : ZRT/ZRTA

Size	Document Number	Rev
	+VGPU_CORE(UP1642PQAG)	2A
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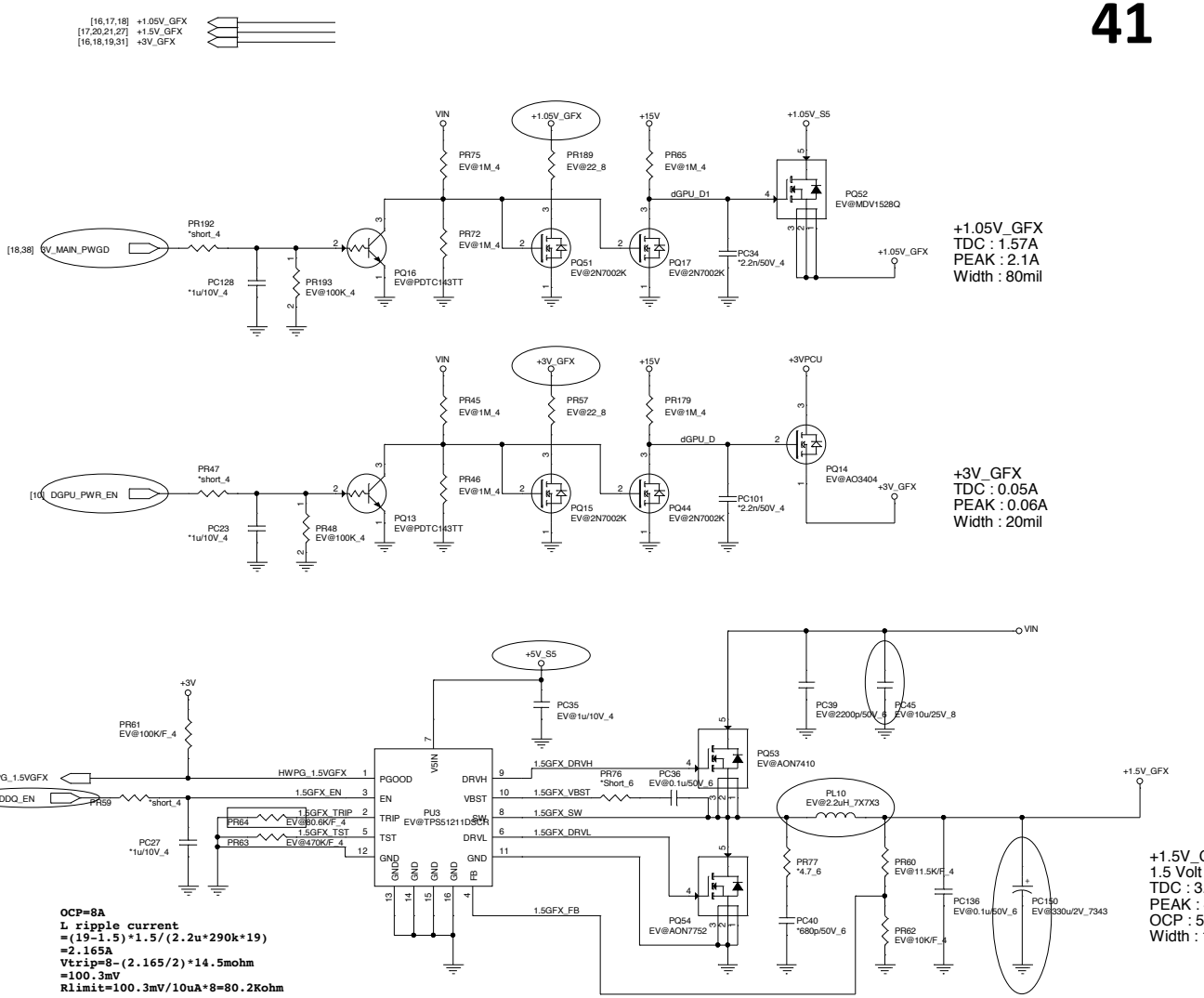

Quanta Computer Inc.		
PROJECT : ZRT/ZRTA		
Size	Document Number: +1.5V_GFX/+1.05V_GFX/+3V_GFX	Rev: 2A
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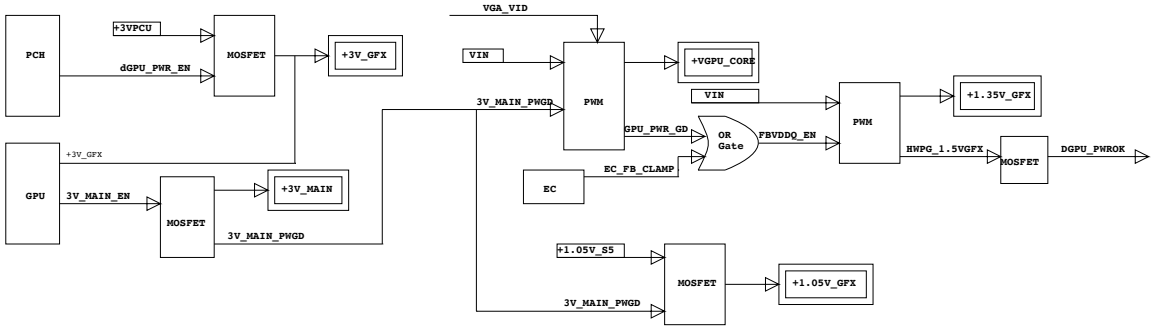
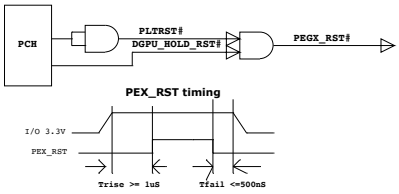
VGA power up sequence



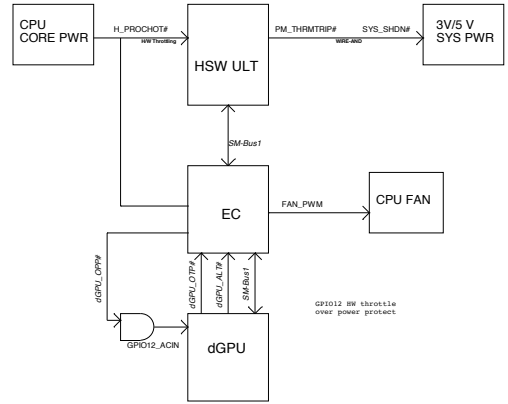
VGA Reset



Power States

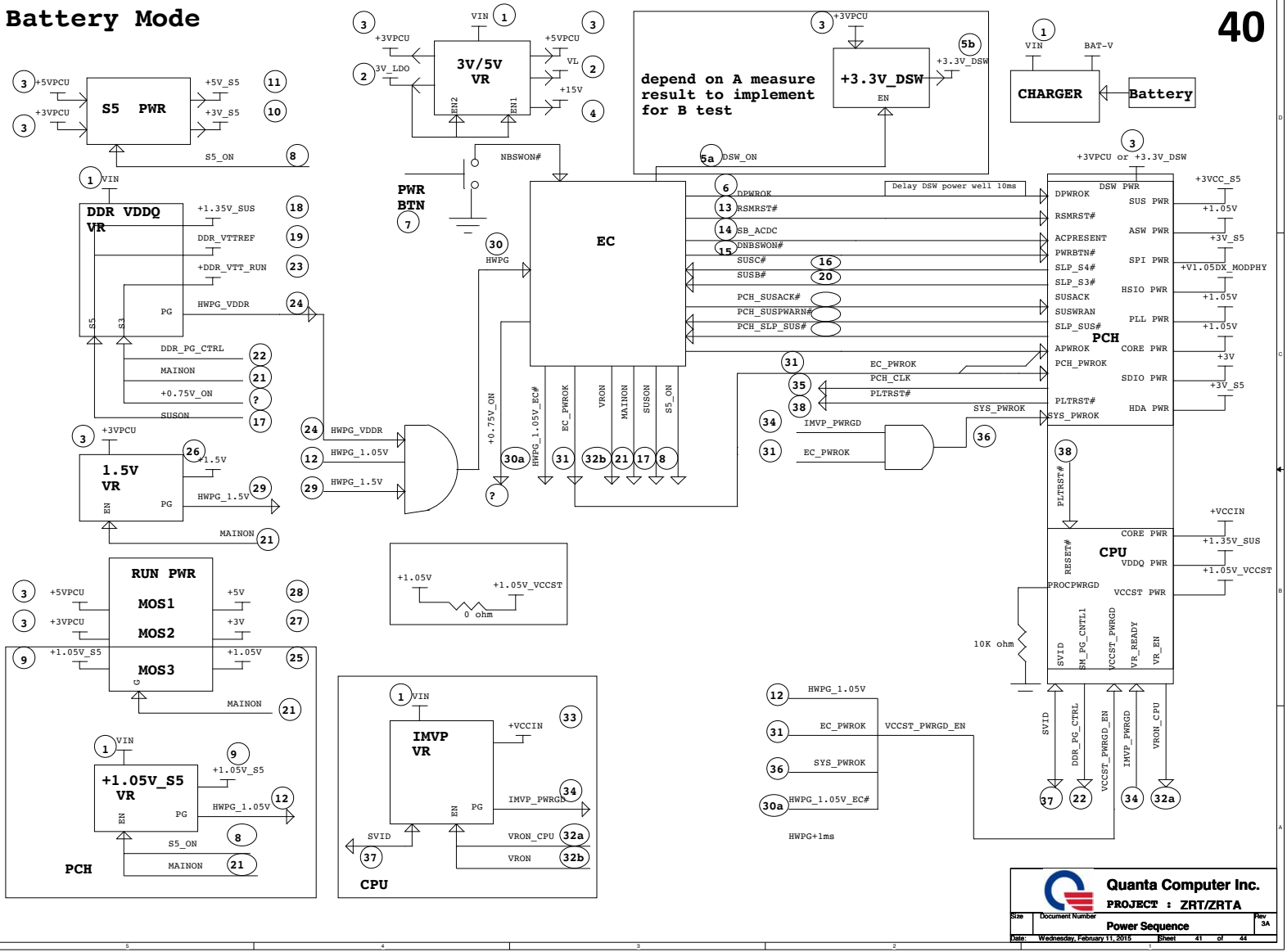
POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+3V_RTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	USB CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/SPK/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.35VSUS	+1.35V	CPU/SODIMM/MD POWER	SUSON	S0-S3
+DDR_VTT_RUN	+0.675V	SODIMM/MD Termination POWER	MAINON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE VCCST POWER	MAINON	S0
+VCCIN	variation	CPU CORE POWER	VRON	S0
+3V_GFX	variation	External GPU POWER	DGPU_PWR_EN	S0
+1.05V_GFX	+3.3V	External GPU POWER	3V_MAIN_EN	S0
+VGPU_CORE	+1.35V	External GPU POWER	3V_MAIN_EN	S0
+1.35V_GFX	+1.05V	External GPU POWER	FBVDDQ_EN	S0

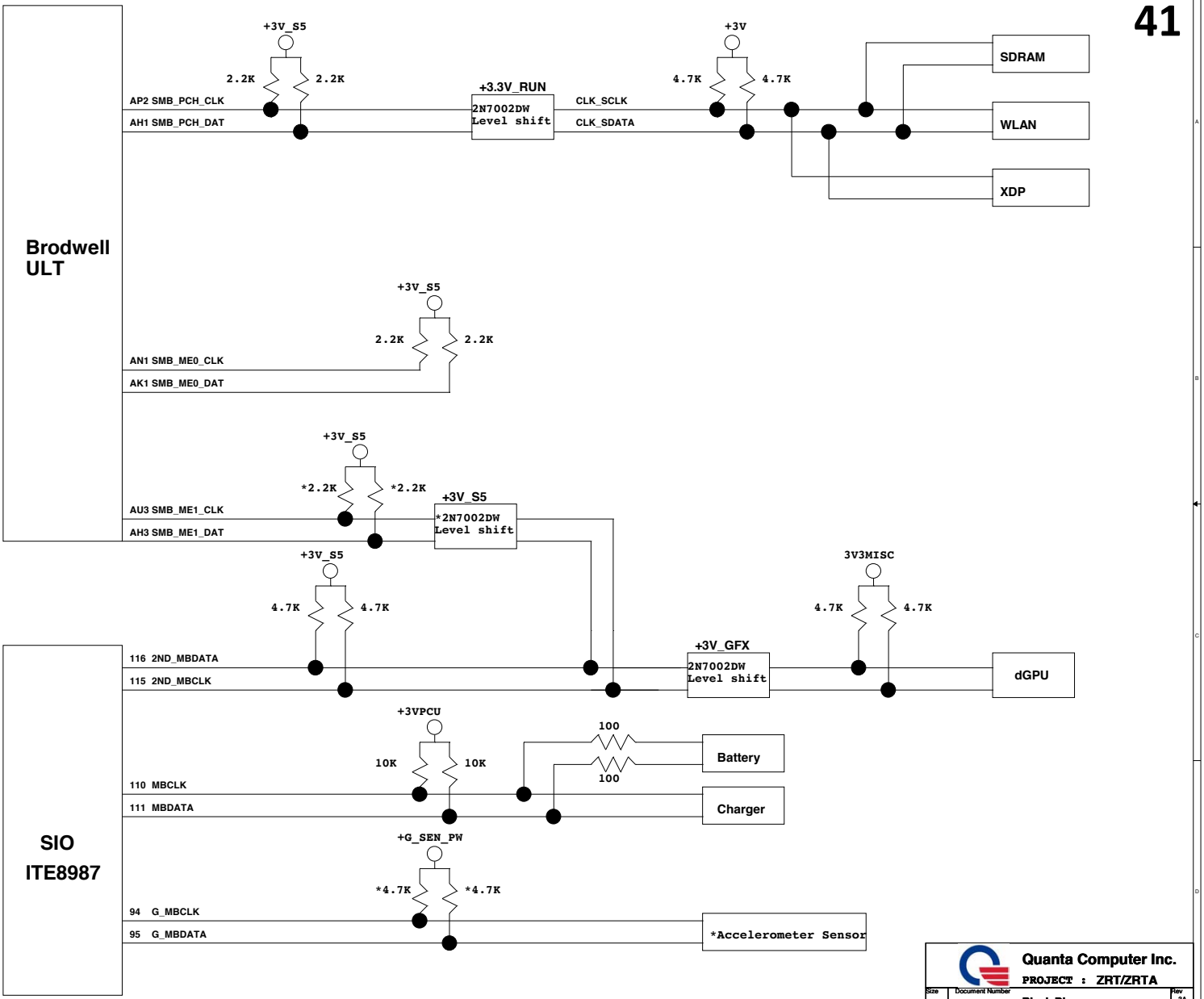
Thermal Follow Chart



dGPU_OPP# EC notify HW throttle over power protect
dGPU_OTP# VGA thrmtrip# => inform EC over temperature protect

Battery Mode





Quanta Computer Inc.
PROJECT : ZRT/ZRTA

Size	Document Number	Rev
	Block Diagram	3A

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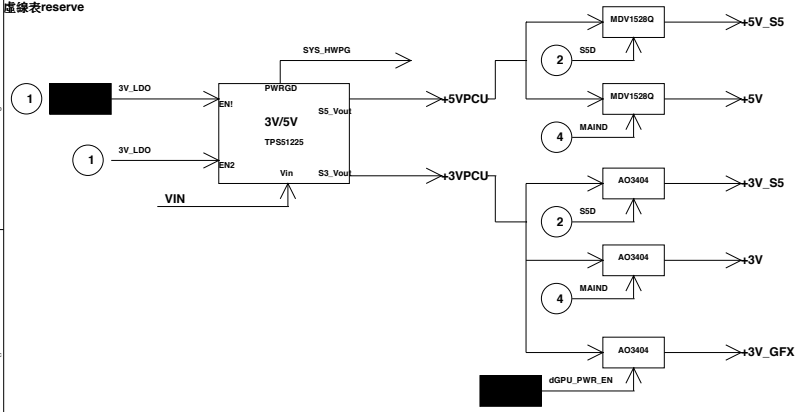
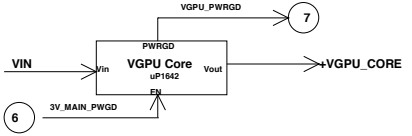
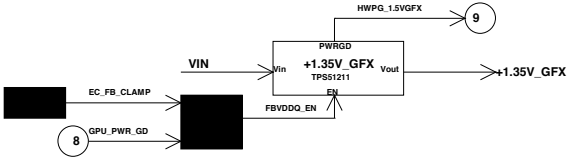
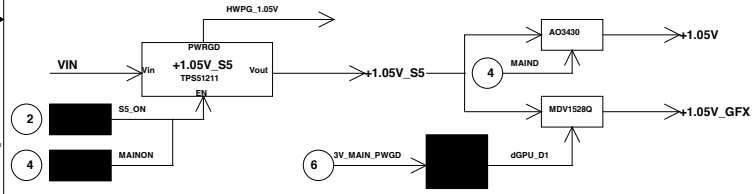
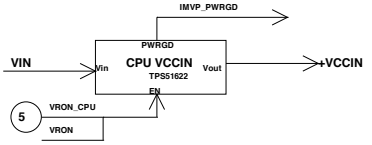
實線表defult
虛線表reserve

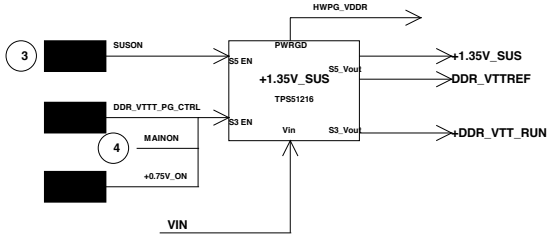


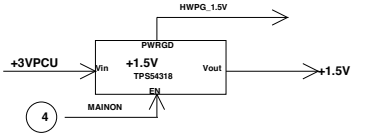












Quanta Computer Inc.
PROJECT : ZRT/ZRTA
ULT PWR CONTROL
Size | Document Number | Rev 3A
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Model	Version	CHANGE LIST	
ZQ0	1A-1	1	2013/10/15 change pin define and add pwm IC.(page31)
		2	2013/10/15 Change VGA ITE solution to NXP.(page 23)
		3	2013/10/15 power board CN change to 6pin.(Page 23)
		4	2013/10/15 U5017.12 change 27M crystal to VGA IC.(Page 23)
		5	2013/10/15 U5017.14 add power rail +3V_RTC(page23)
		6	2013/10/15 strap0 R672 DG 50k PU.(Page 19)
		7	2013/10/15 Change AND gat to Q63 D-MOS.(Page 19)
		8	2013/10/15 change pin define and add pwm IC U17.(Page 46)
		9	2013/10/15 for GC6 stuff R228\R1013\R226\R1012.un-stuff Q24\Q26\R227\R1011. (Page19)
		10	20131015 For GC6 NV DG GC6_FB_EN PD.(Page10)
		11	2013/10/15 following up acer define and swap USB3 and USB2 port.(Page9)
		12	2013/10/15 swap CAP C8579/C8580 to Vrefo and resistor R5214/R5215 to Line in.(Page30)
		13	2013/10/15 U27.30/U27.31 del fan Pwm signal.(Page32)
		14	20131015 change LVDS\USB3\RJ45\FAN\TPD\USB DB CN\DC-IN CN\Power Button\Cardreader\KB BLK CN\Power board, footprint.
	1A-2	1	2013/10/16 JDIM5 Swap M_B_DQS2/M_B_DQS3 and swap M_B_DQS#2/M_B_DQS#3.(page15)
		2	2013/10/16 JDIM6 Chage net name M_B_DQS#[7:0] to M_A_DQS#[7:0].(page14)
		3	2013/10/16 Add RTC charge circuit.(page8)
		4	2013/10/16 BT1.1 Chage +3V_RTC_0 to VCCTC_2.(page8)
		5	2013/10/15 change power rail from +3V_RTC_0 to VCCRTC_2.(page23)